Nailgun: Breaking the Privilege Isolation on ARM

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Sep 23, 2019

Outline

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- Background
- Introduction
- Obstacles for Misusing the Traditional Debugging
- Nailgun Attack
- Mitigations
- Conclusion

Outline

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Breaking the Privilege Isolation on ARM

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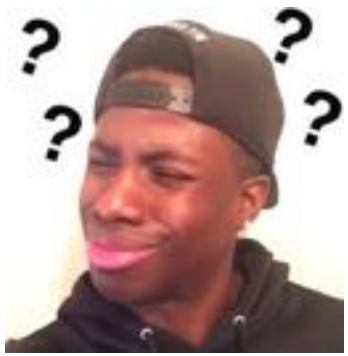
Breaking the Privilege Isolation on ARM



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Breaking the Privilege Isolation on ARM

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What is ARM?

- **In Dictionary**: Hands, or weapons.
- **Company**: ARM was a British semiconductor company, now owned by SoftBank.
- **Architecture**: ARM is a processor architecture designed by ARM company.

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Privilege Isolation

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What is Privilege Isolation?

- **Privilege In Dictionary**: A special right, advantage, or immunity granted or available only to a particular person or group.
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Privilege Isolation

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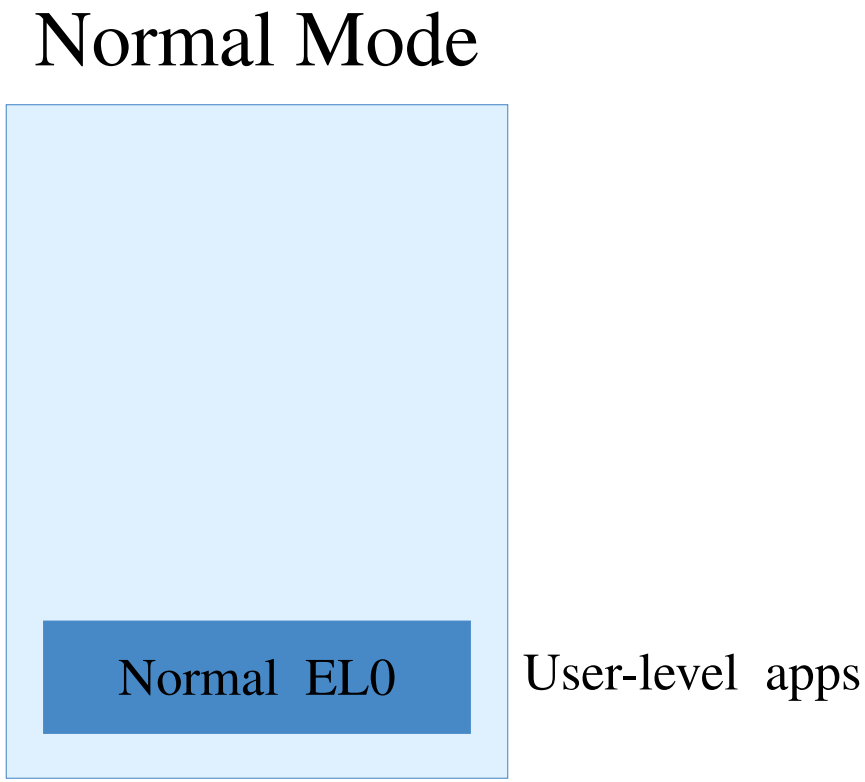
Exception Levels in ARM:

- **Exception**: is used to divert the normal execution control flow, to allow the processor to handle internal or external events.
- **Exception Levels**: are used to specify different privileges in ARM processor.

Privilege Isolation



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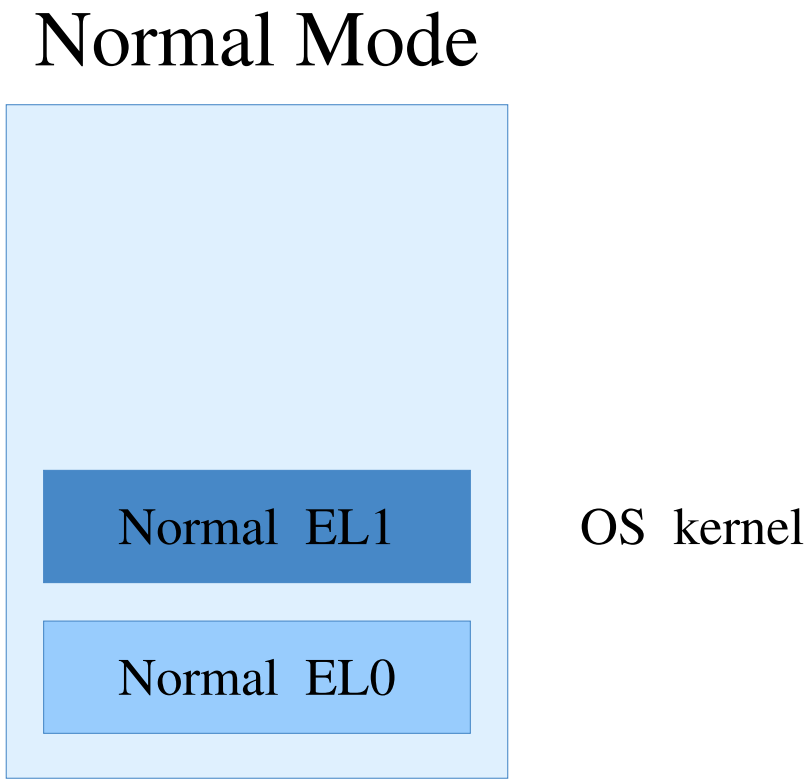

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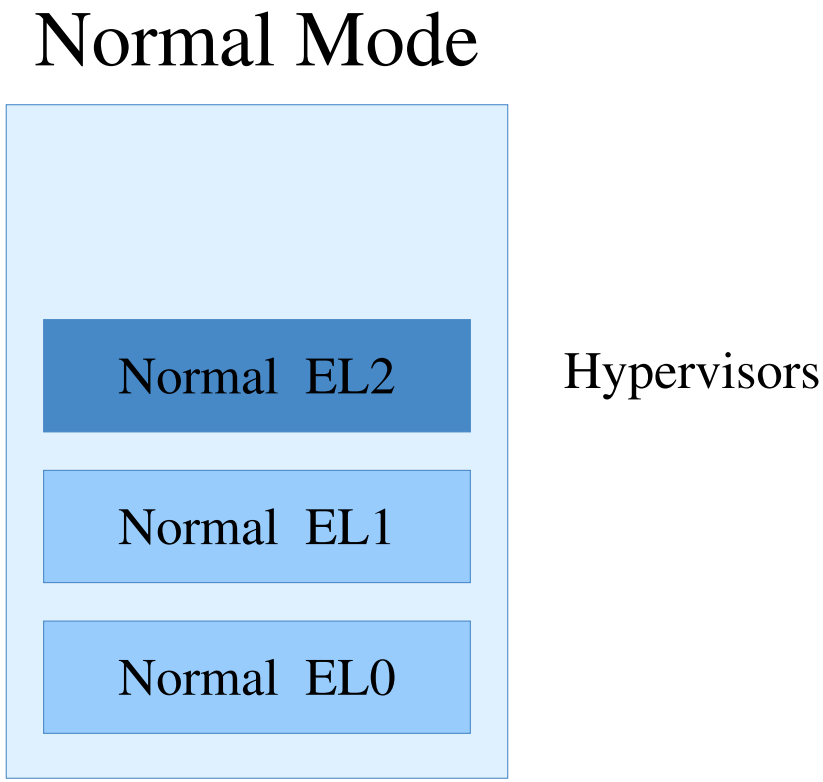

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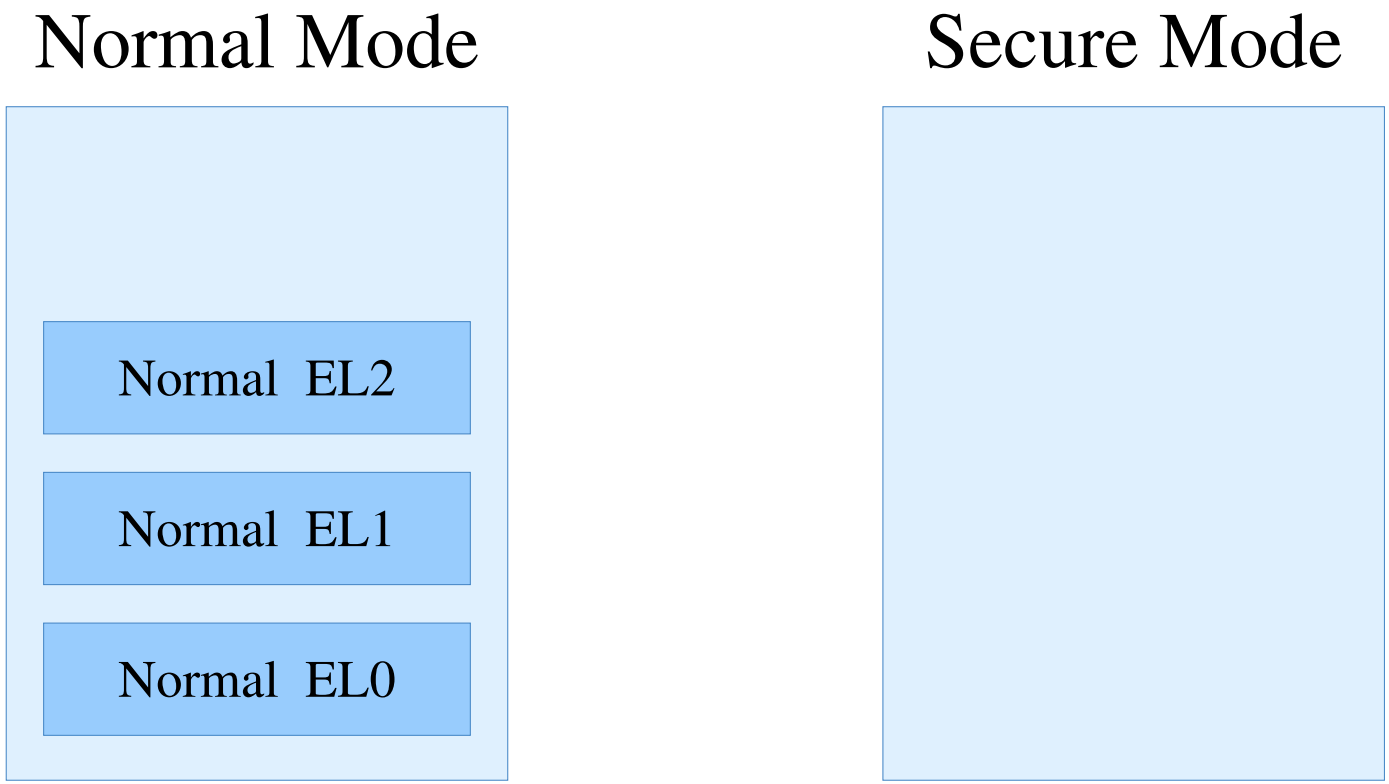

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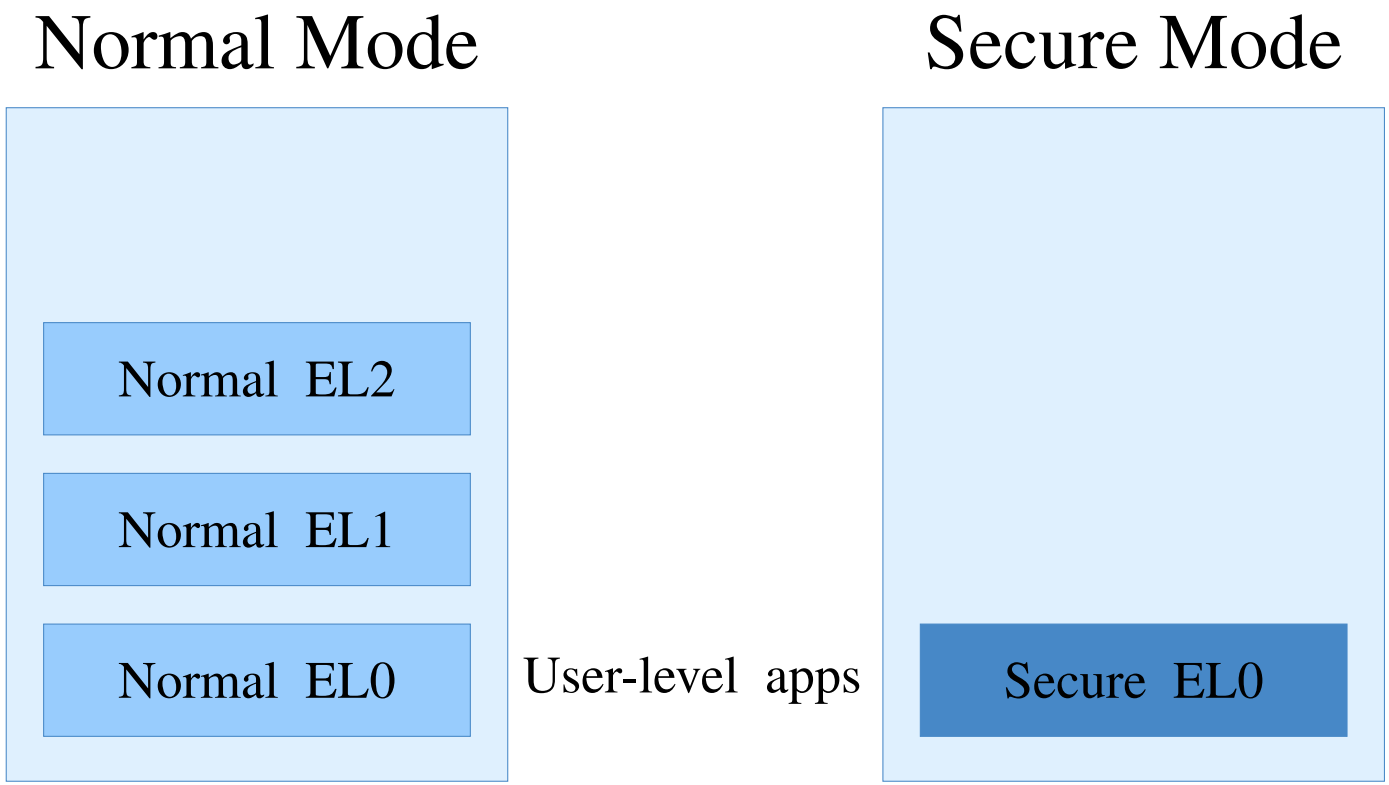

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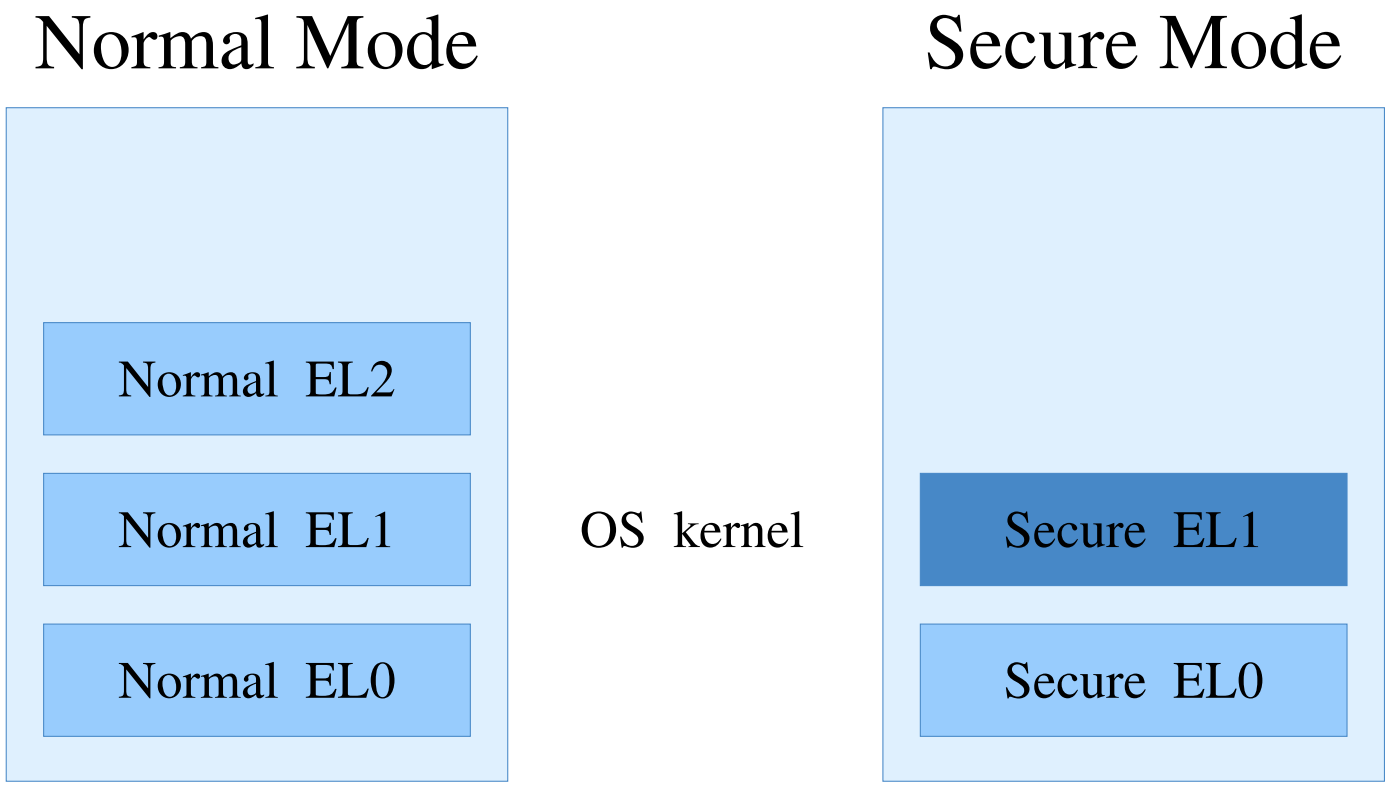

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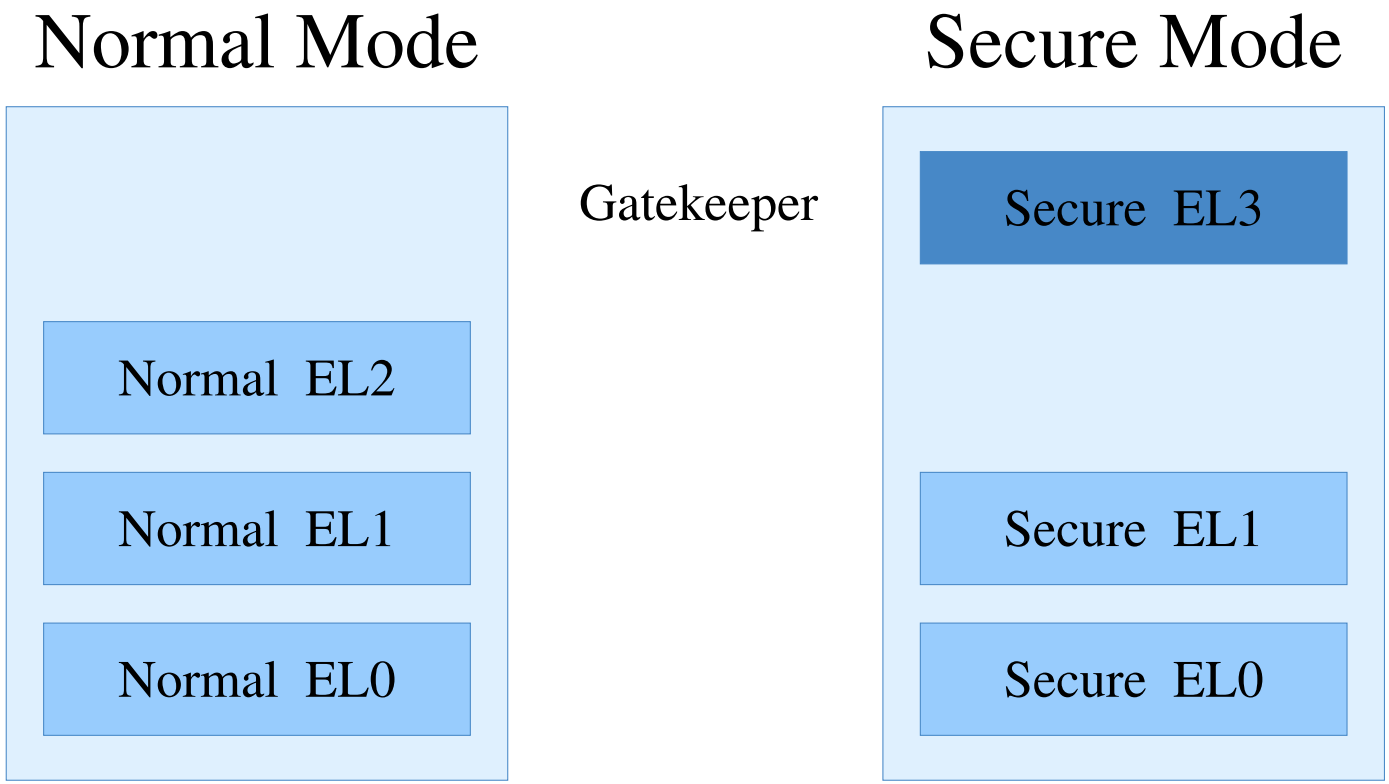

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Breaking the Privilege Isolation on ARM

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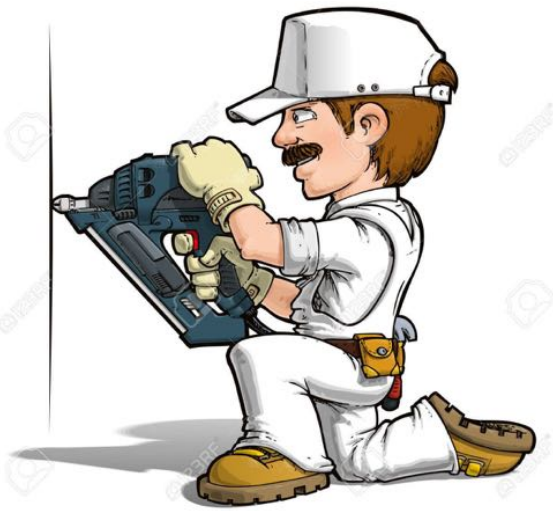

Figure source: https://www.123rf.com/

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Introduction

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Modern processors are equipped with hardware-based debugging features to facilitate on-chip debugging process.

- E.g., hardware breakpoints and hardware-based trace.

- It normally requires cable connection (e.g., JTAG [1]) to make use of these features.

Traditional Debugging

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Debug Target
(TARGET)

Security?

Traditional Debugging

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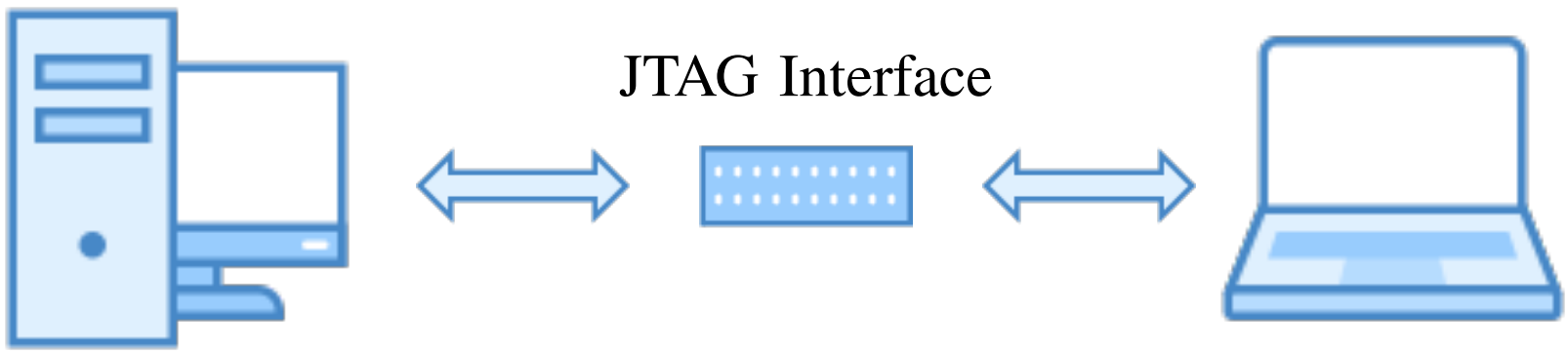
Debug Target
(TARGET)

Debug Host
(HOST)

Security?

Traditional Debugging



Security?

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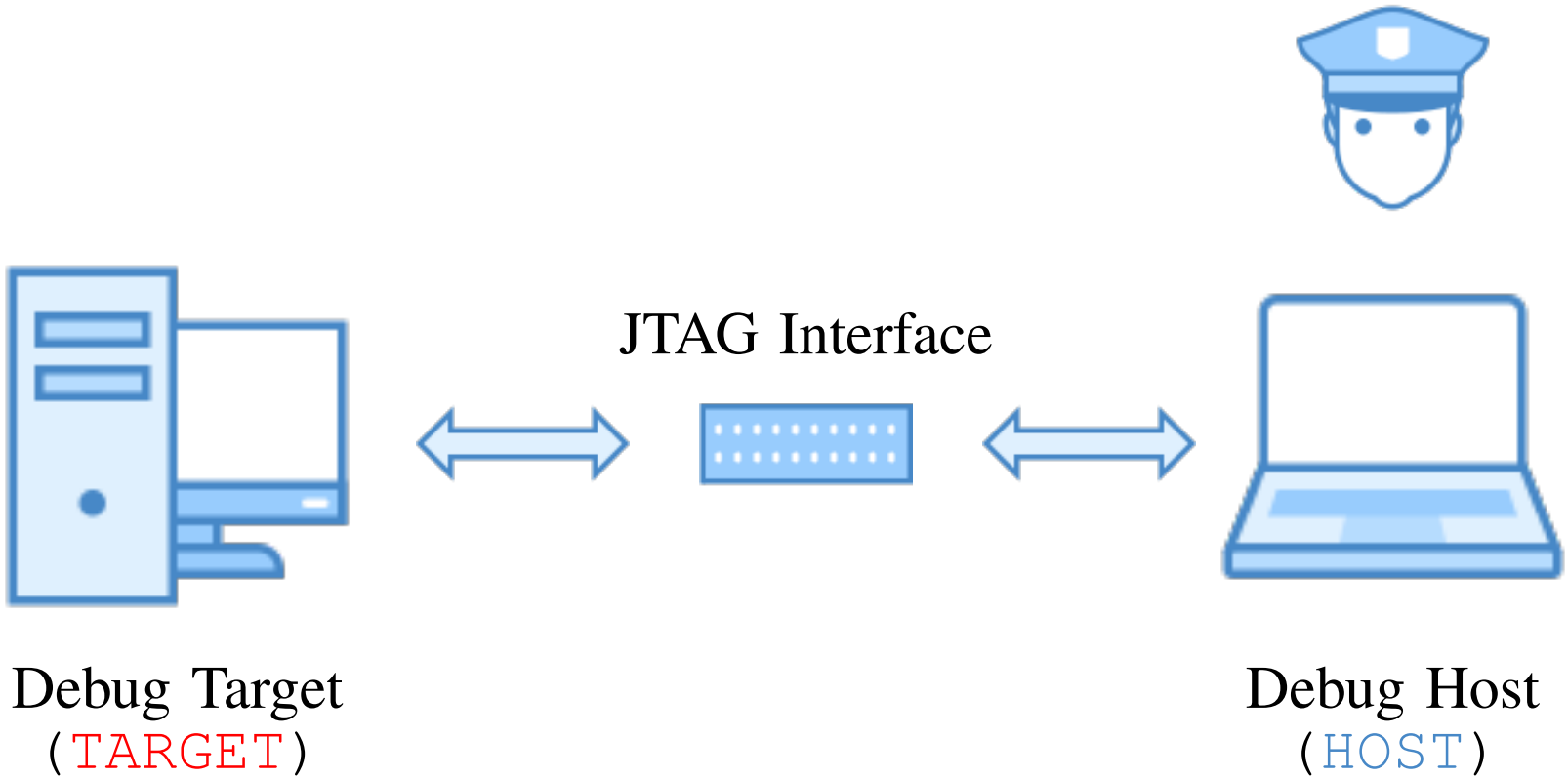

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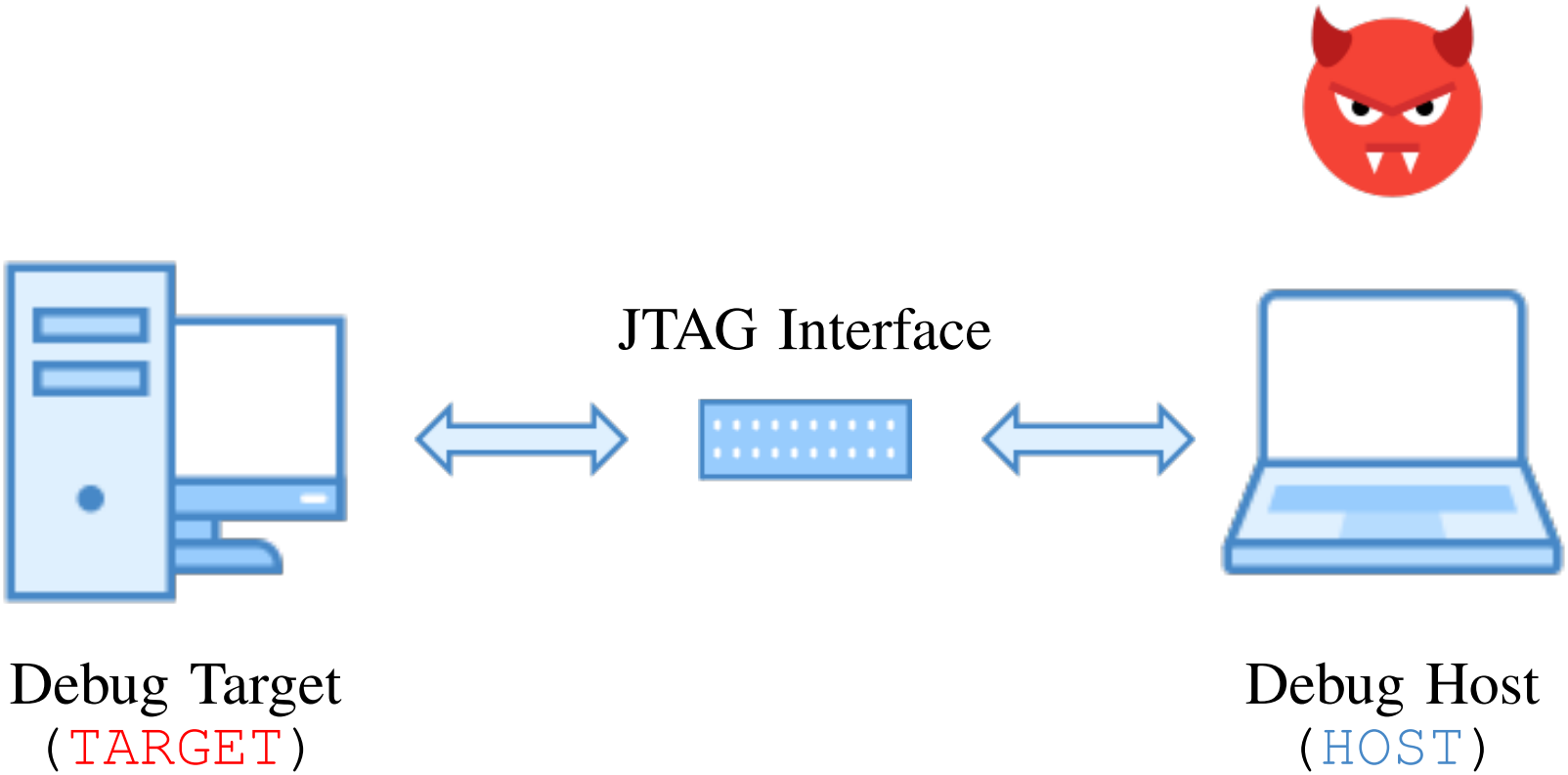

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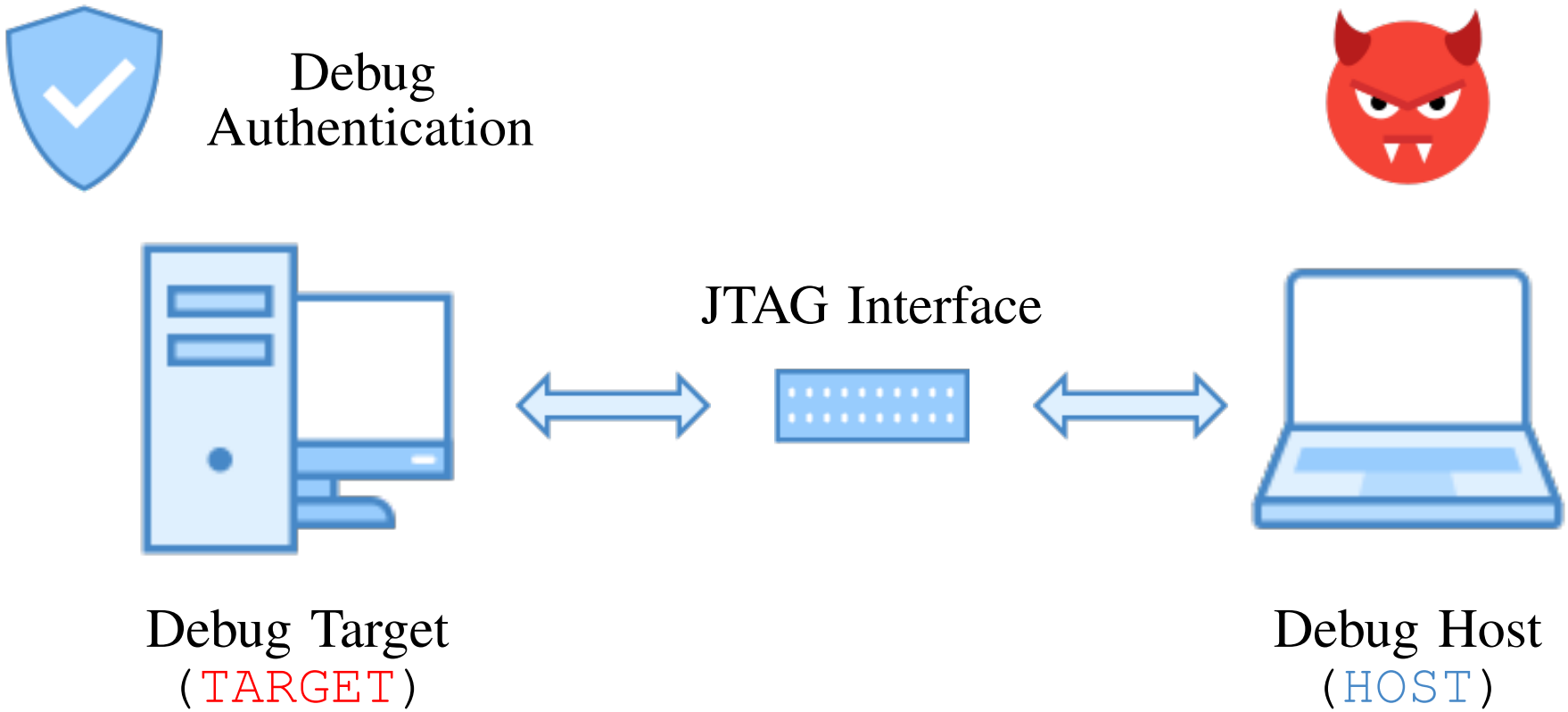
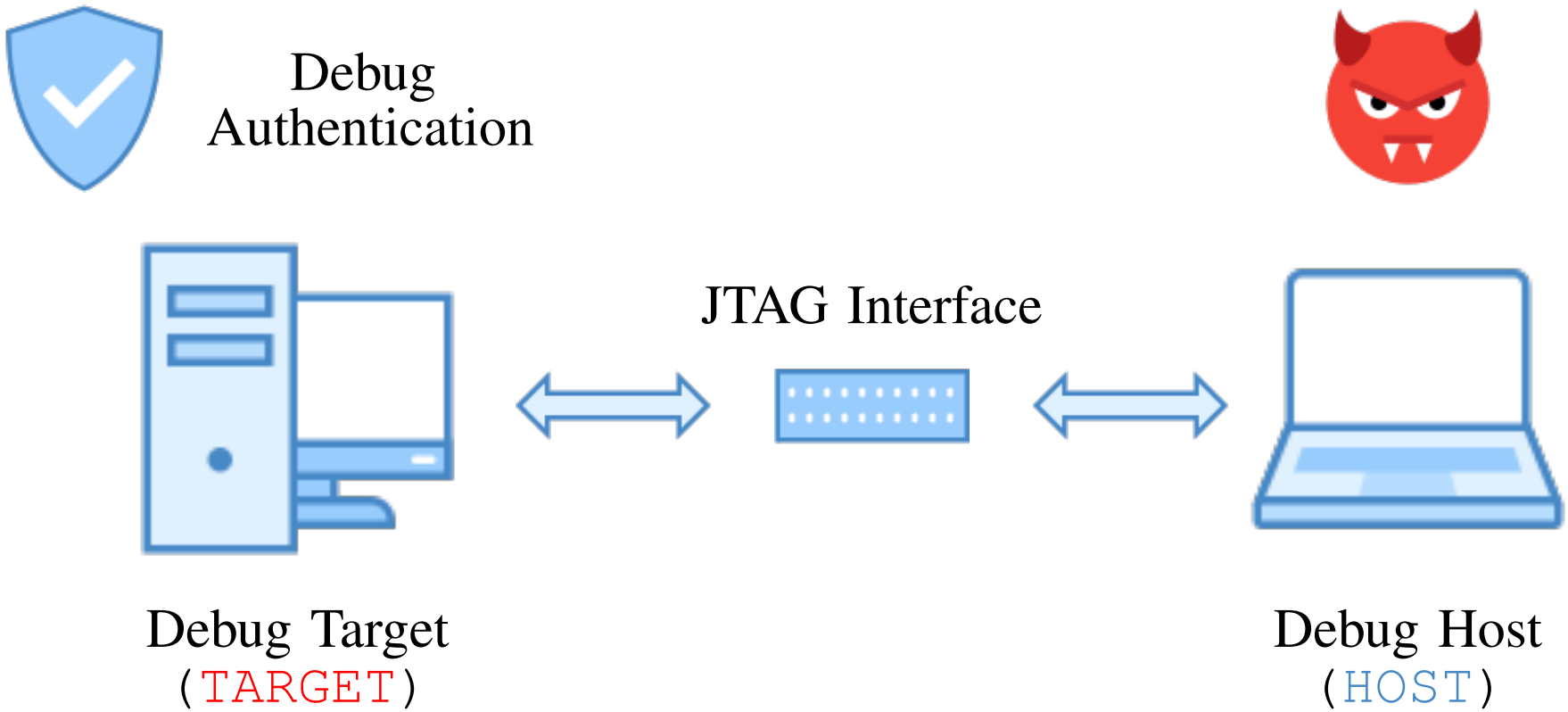


Security?

Traditional Debugging



Security?

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Security? We have obstacles for attackers!

- **Obstacle 1**: Physical access.
- **Obstacle 2**: Debug authentication mechanism.

Do these obstacles work?

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Do these obstacles work?

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Obstacles for Misusing the Traditional Debugging

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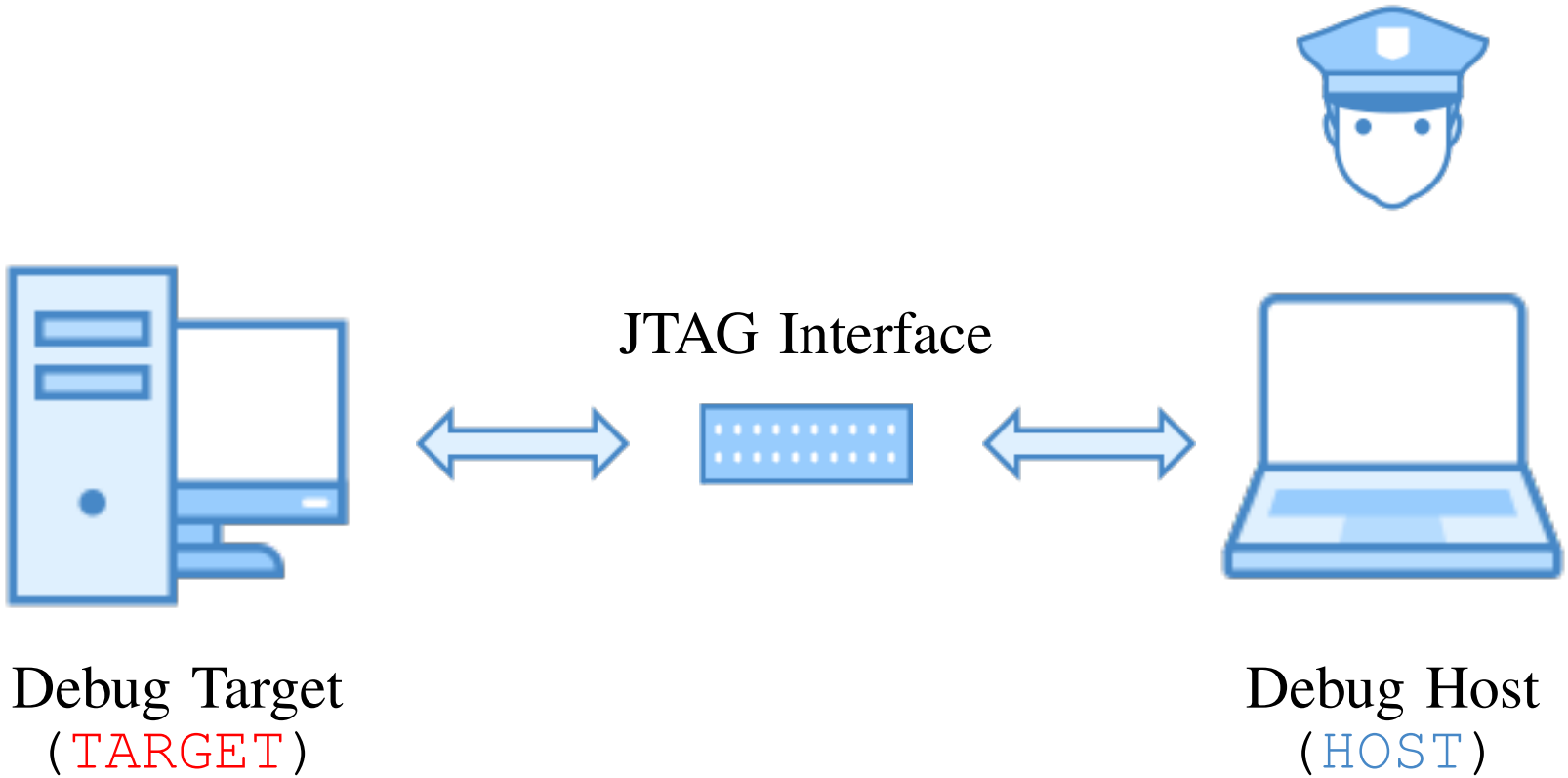
Obstacles for attackers:

- **Obstacle 1**: Physical access.
- **Obstacle 2**: Debug authentication mechanism.

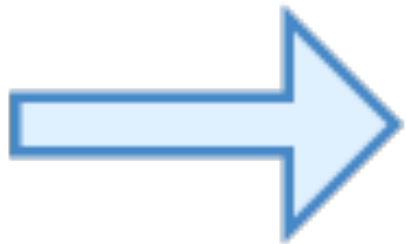
Does it really require physical access?

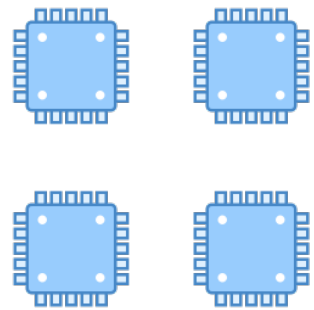
Traditional Debugging



Traditional Debugging

Debug Target
(TARGET)





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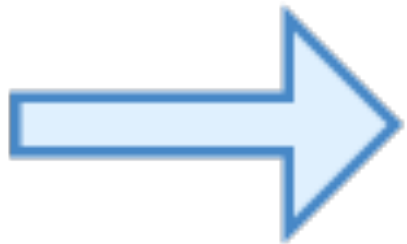

Traditional Debugging

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Use one to debug another one?

Inter-Processor Debugging

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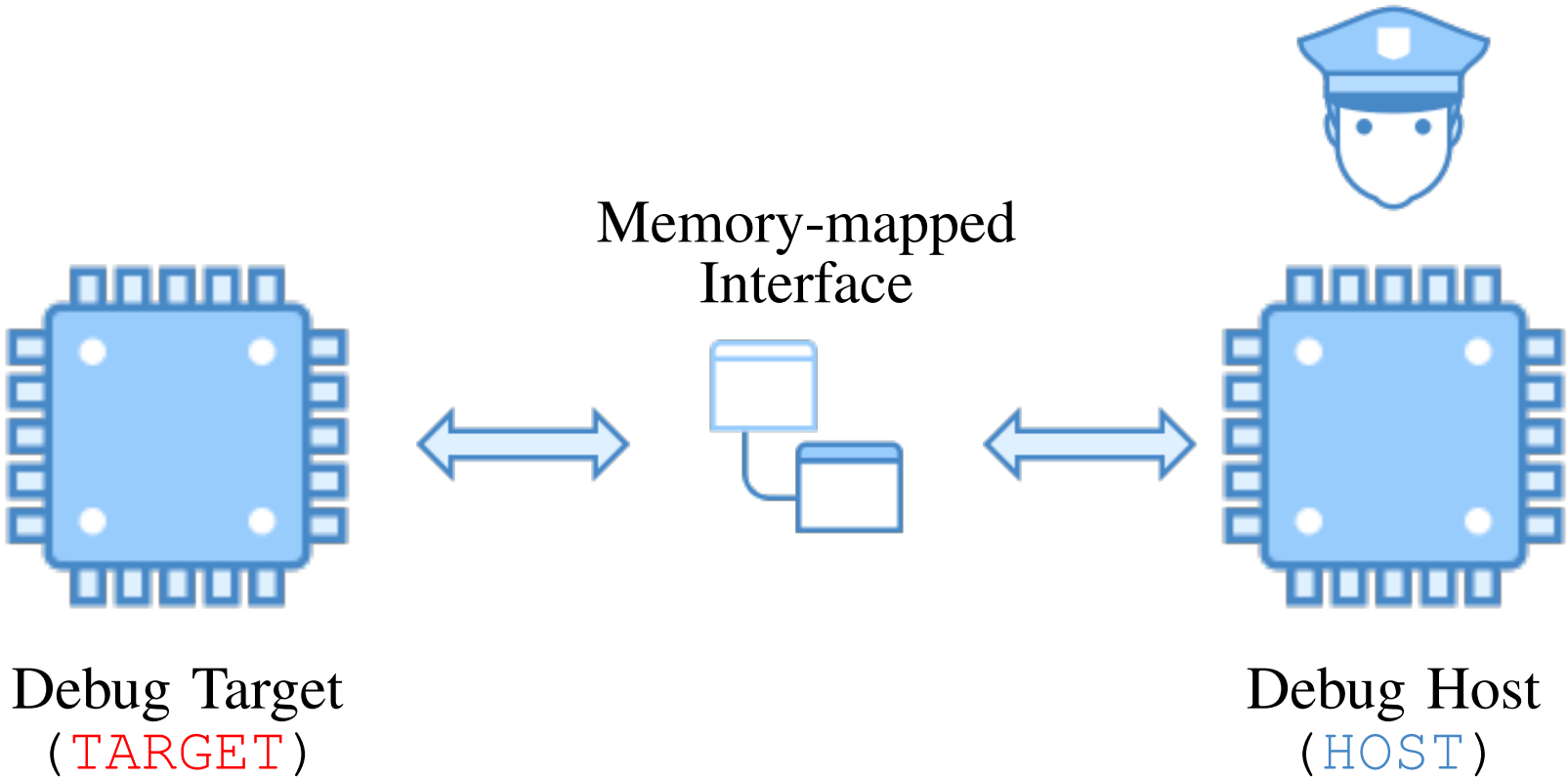
We can use one processor on the chip to debug another one on the same chip, and we refer it as `inter-processor debugging`.

- Memory-mapped debugging registers.
  - Introduced since ARMv7.

- No JTAG, No physical access.

Inter-Processor Debugging



Obstacles for Misusing the Traditional Debugging

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Obstacles for attackers:

- **Obstacle 1**: Physical access.
- **Obstacle 2**: Debug authentication mechanism.

Does debug authentication work as expected?

Processor in Normal State

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`TARGET` is executing instructions pointed by `pc`

Processor in Non-invasive Debugging

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Non-invasive Debugging: Monitoring without control

Processor in Invasive Debugging

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Invasive Debugging: Control and change status

ARM Debug Authentication Mechanism

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Debug Authentication Signal: Whether debugging is allowed

ARM Debug Authentication Mechanism

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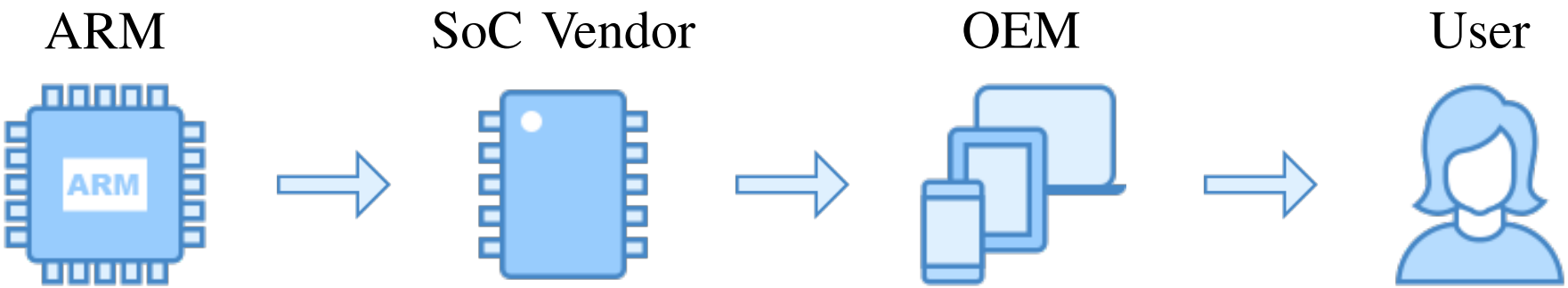
Four signals for: Secure/Non-secure, Invasive/Non-invasive

ARM Ecosystem



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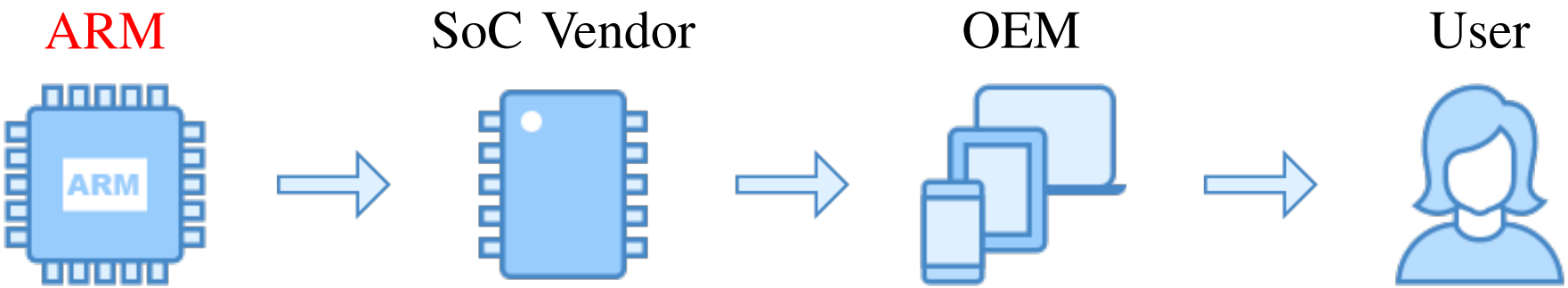
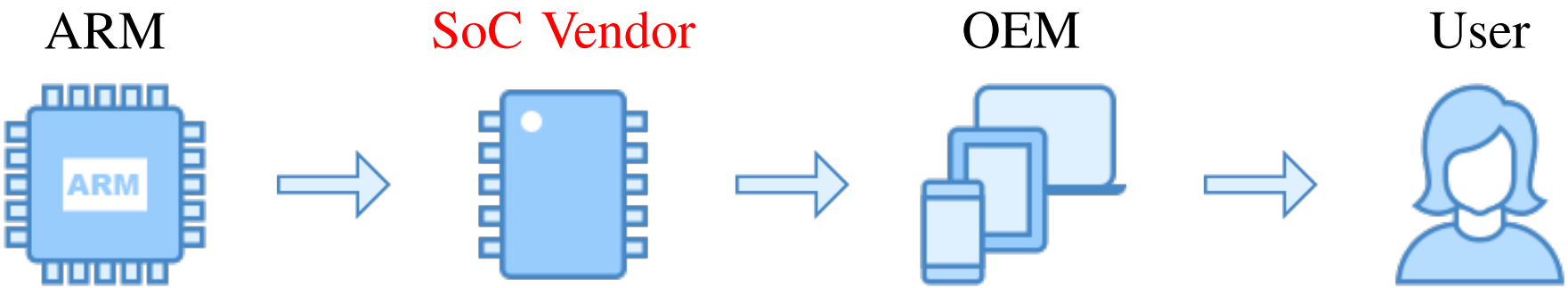


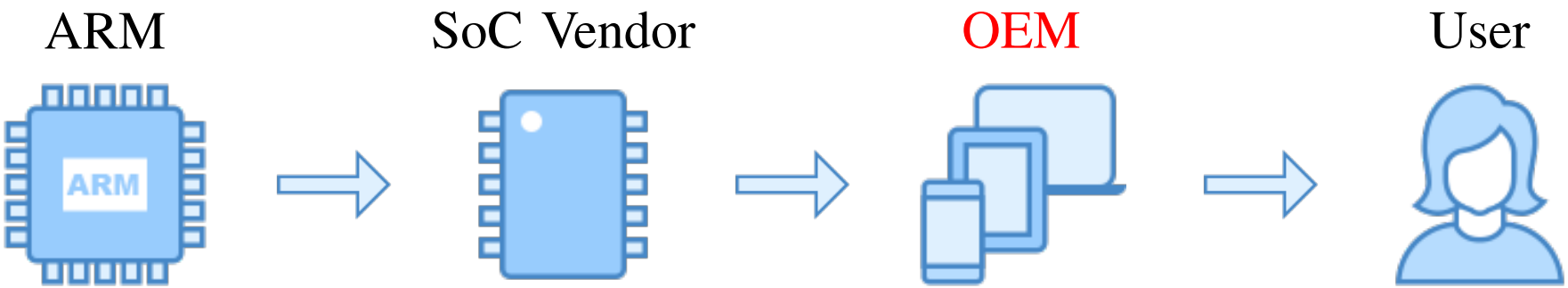
- ARM licenses technology to the System-On-Chip (SoC) Vendors.
  - E.g., ARM architectures and Cortex processors
- **Defines** the debug authentication signals.

ARM Ecosystem



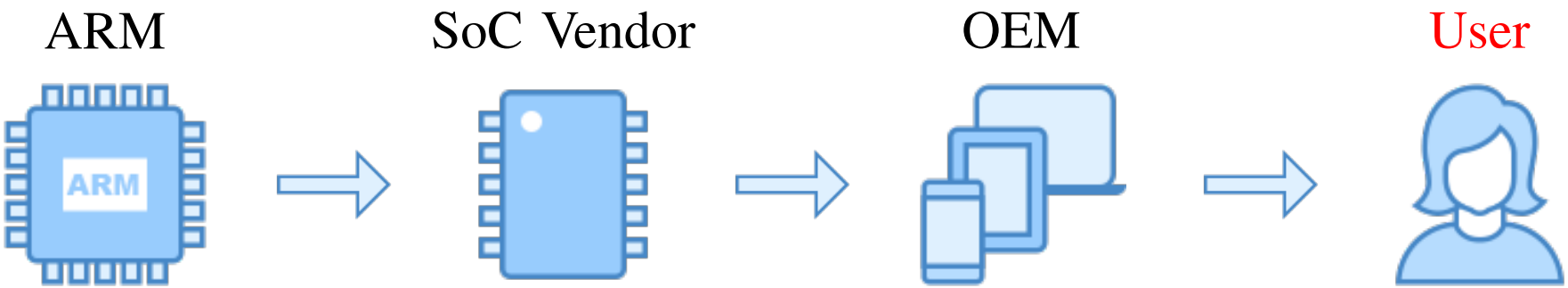
- The SoC Vendors develop chips for Original Equipment Manufacturers (OEMs).
  - E.g., Qualcomm Snapdragon SoCs
- **Implement** the debug authentication signals.

ARM Ecosystem



- The OEMs produce devices for the users.
  - E.g., Samsung Galaxy Series and Huawei Mate Series
- **Configure** the debug authentication signals.

ARM Ecosystem



- Finally, the User can enjoy the released devices.
  - Tablets, smartphones, and other devices
- **Learn** the status of debug authentication signals.

Obstacles for Misusing the Traditional Debugging

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Obstacles for attackers:

- **Obstacle 1**: Physical access.
- **Obstacle 2**: Debug authentication mechanism.

Does debug authentication work as expected?

Debug Authentication Signals

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- What is the status of the signals in real-world device?
- How to manage the signals in real-world device?

Debug Authentication Signals

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Table: Debug Authentication Signals on Real Devices.

Category	Platform / Device	Debug Authentication Signals			
		DBGEN	NIDEN	SPIDEN	SPNIDEN
Development Boards	ARM Juno r1 Board	✔	✔	✔	✔
	NXP i.MX53 QSB	✖	✔	✖	✖
IoT Devices	Raspberry PI 3 B+	✔	✔	✔	✔
Cloud Platforms	64-bit ARM miniNode	✔	✔	✔	✔
	Packet Type 2A Server	✔	✔	✔	✔
	Scaleway ARM C1 Server	✔	✔	✔	✔
Mobile Devices	Google Nexus 6	✖	✔	✖	✖
	Samsung Galaxy Note 2	✔	✔	✖	✖
	Huawei Mate 7	✔	✔	✔	✔
	Motorola E4 Plus	✔	✔	✔	✔
	Xiaomi Redmi 6	✔	✔	✔	✔

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	Packet Type 2A Server	✔	✔	✔	✔
	Scaleway ARM C1 Server	✔	✔	✔	✔
Mobile Devices	Google Nexus 6	✖	✔	✖	✖
	Samsung Galaxy Note 2	✔	✔	✖	✖
	Huawei Mate 7	✔	✔	✔	✔
	Motorola E4 Plus	✔	✔	✔	✔
	Xiaomi Redmi 6	✔	✔	✔	✔

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	Packet Type 2A Server	✔	✔	✔	✔
	Scaleway ARM C1 Server	✔	✔	✔	✔
Mobile Devices	Google Nexus 6	✖	✔	✖	✖
	Samsung Galaxy Note 2	✔	✔	✖	✖
	Huawei Mate 7	✔	✔	✔	✔
	Motorola E4 Plus	✔	✔	✔	✔
	Xiaomi Redmi 6	✔	✔	✔	✔

Debug Authentication Signals

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How to manage the signals in real-world device?

- For both development boards with manual, we cannot fully control the debug authentication signals.
  - Signals in i.MX53 QSB can be enabled by JTAG.
  - The DBGEN and NIDEN in ARM Juno board cannot be disabled.
- In some mobile phones, we find that the signals are controlled by One-Time Programmable (OTP) fuse.

For all the other devices, nothing is publicly available.

Obstacles for Misusing the Traditional Debugging

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Obstacles for attackers:

- ~~**Obstacle 1**: Physical access.~~
  We don't need physical access to debug a processor.

- ~~**Obstacle 2**: Debug authentication mechanism.~~
  The debug authentication mechanism allows us to debug the processor.

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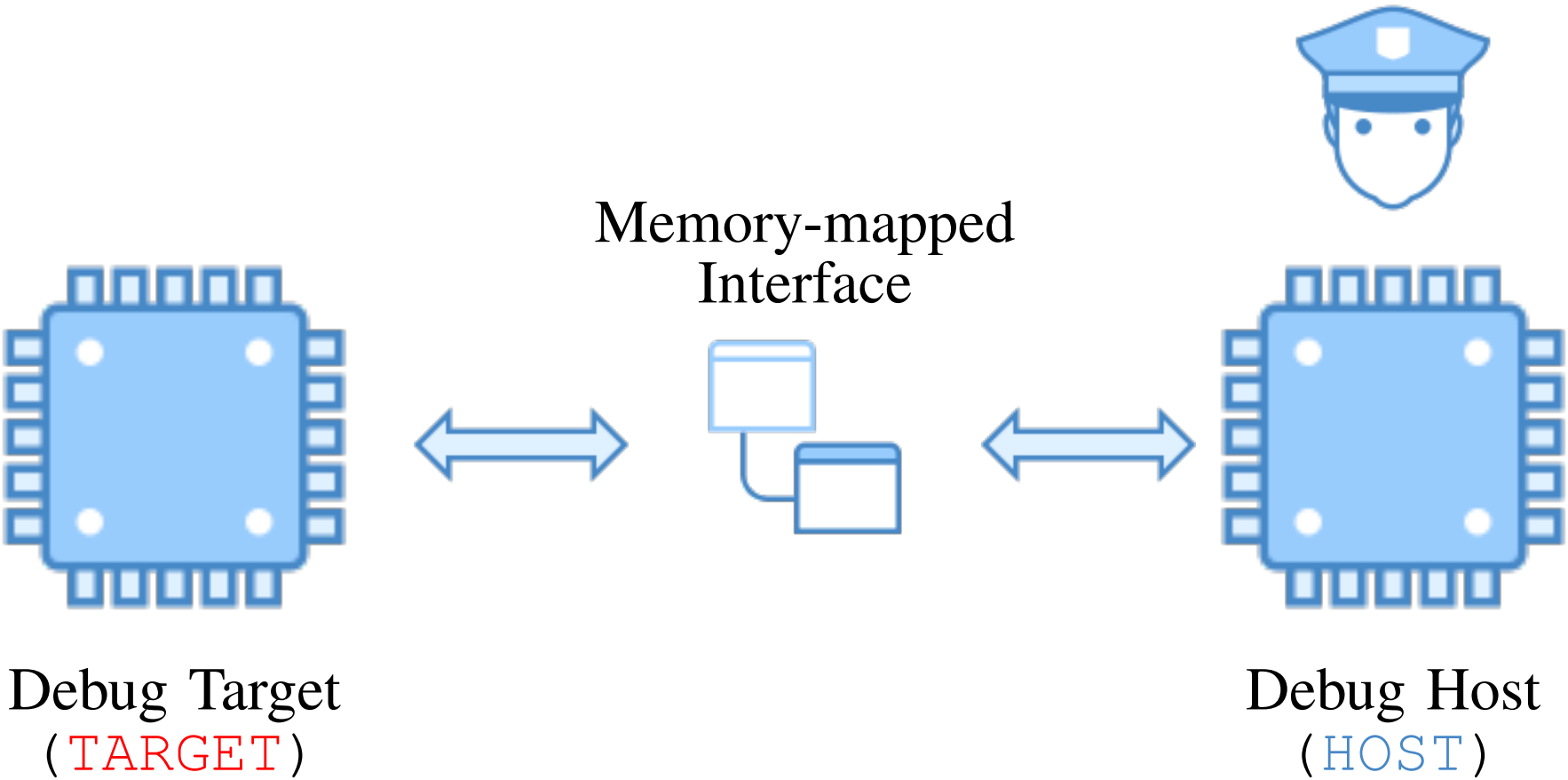
Inter-processor Debugging



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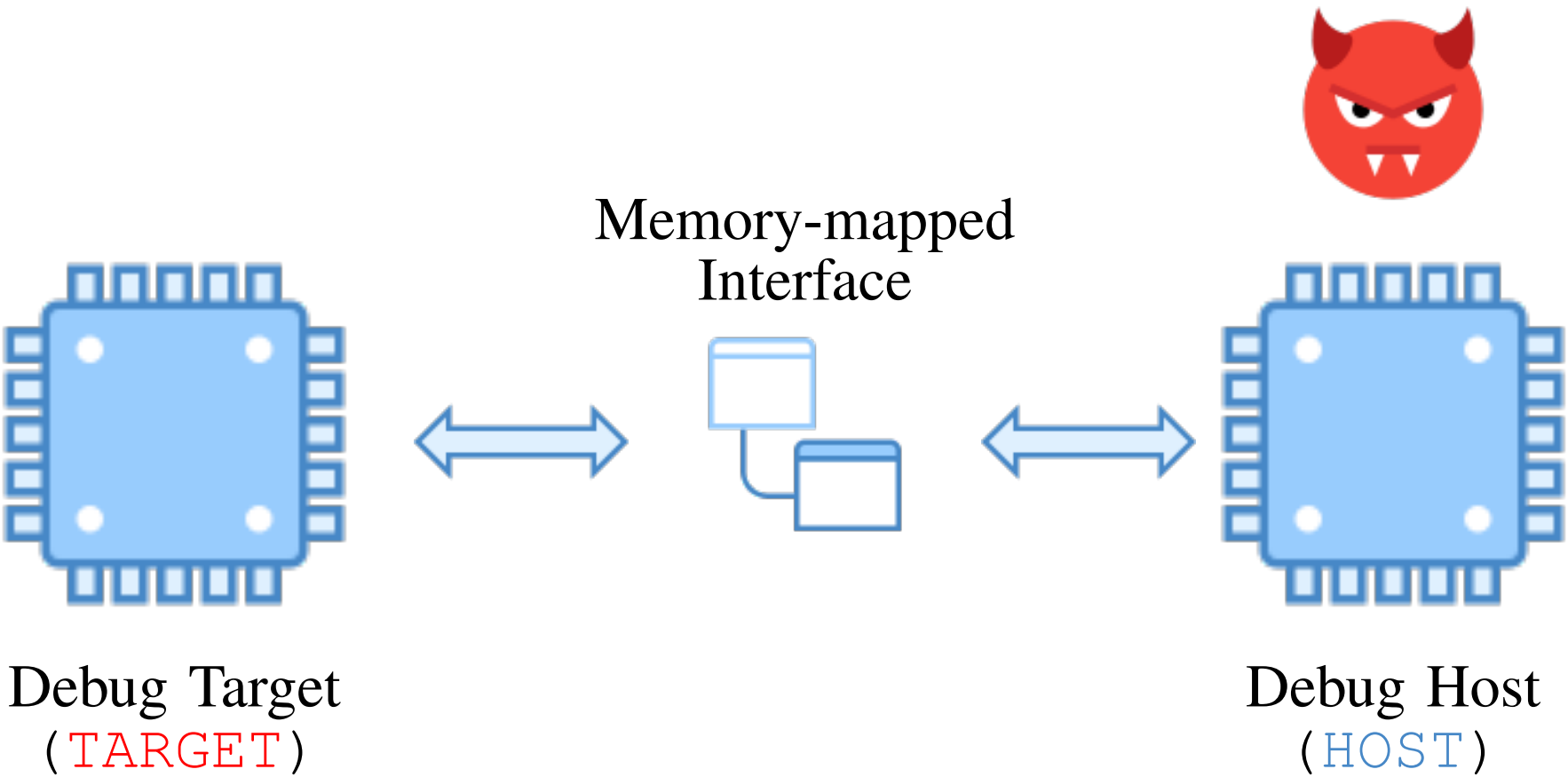
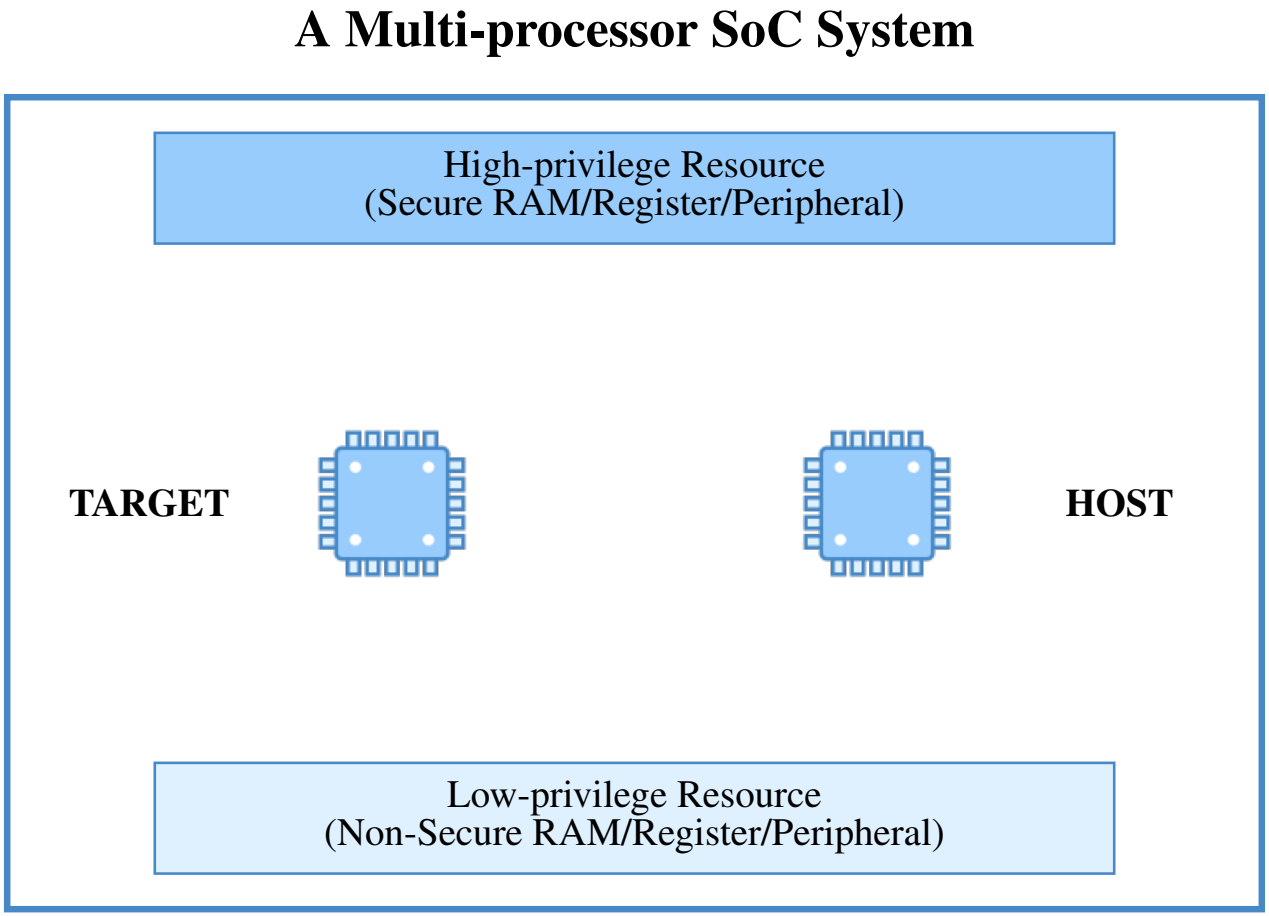


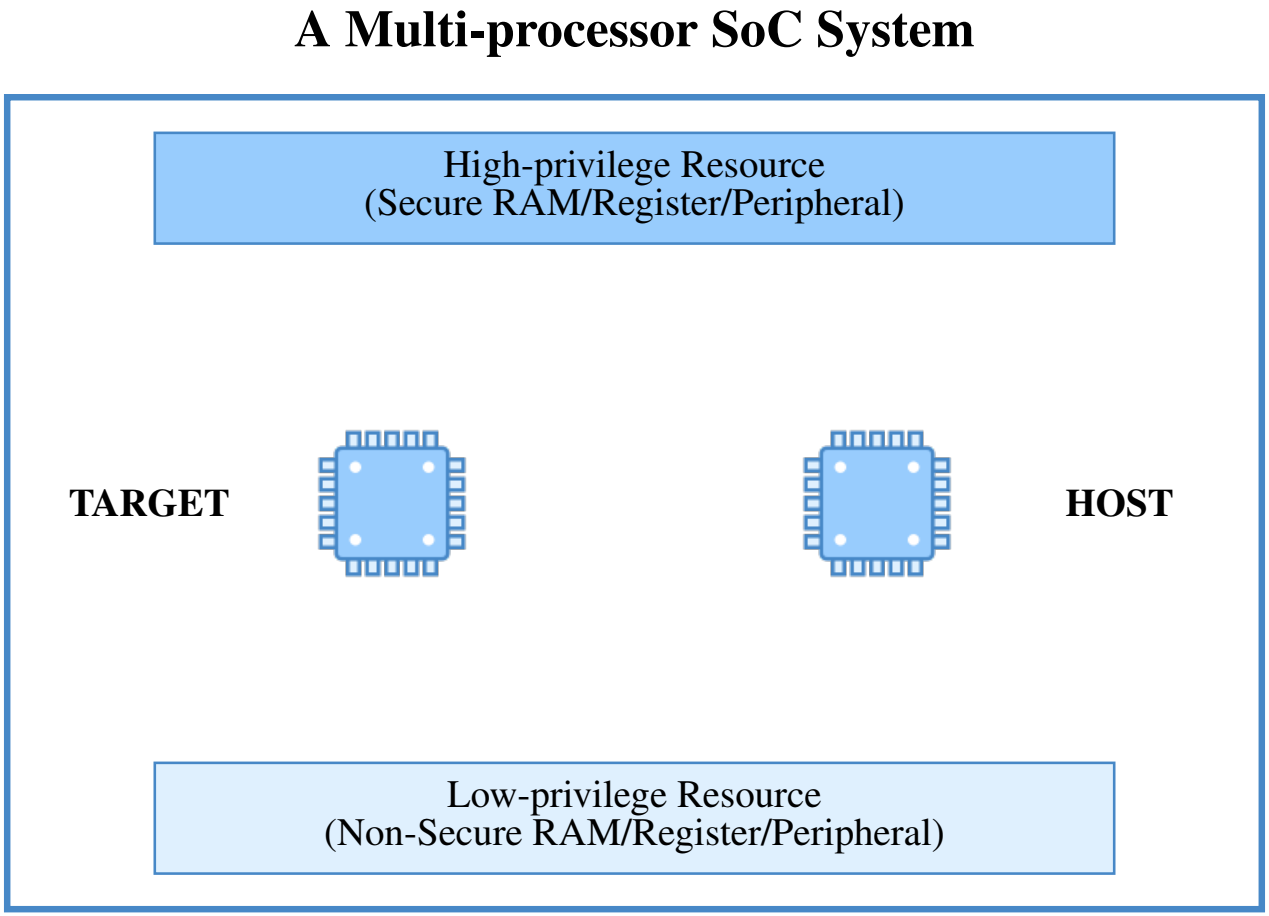
Nailgun Attack



An example SoC system:

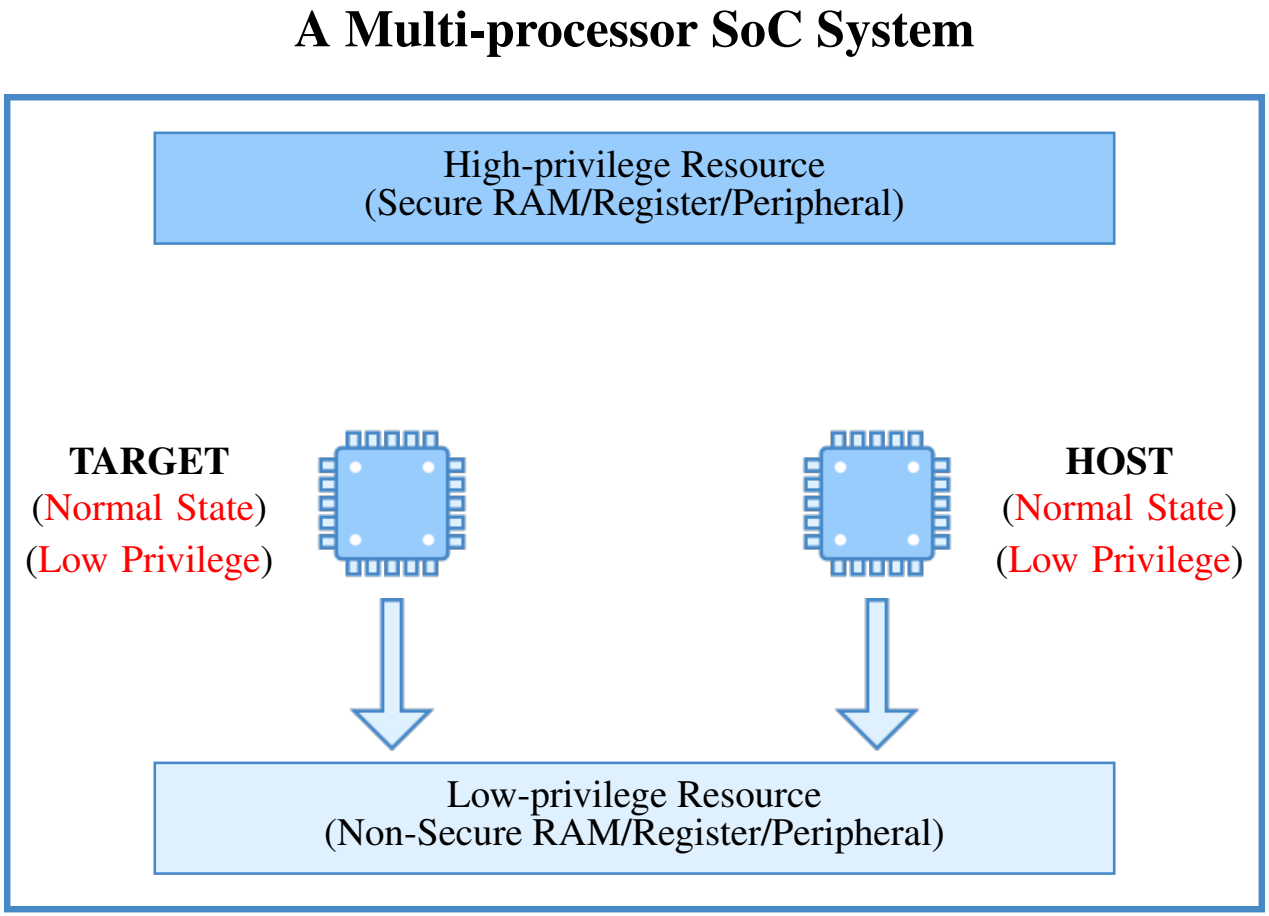
- Two processors as `HOST` and `TARGET`, respectively.
- Low-privilege and High-privilege resource.

Nailgun Attack



- Low-privilege refers to non-secure kernel-level privilege
- High-privilege refers to any other higher privilege

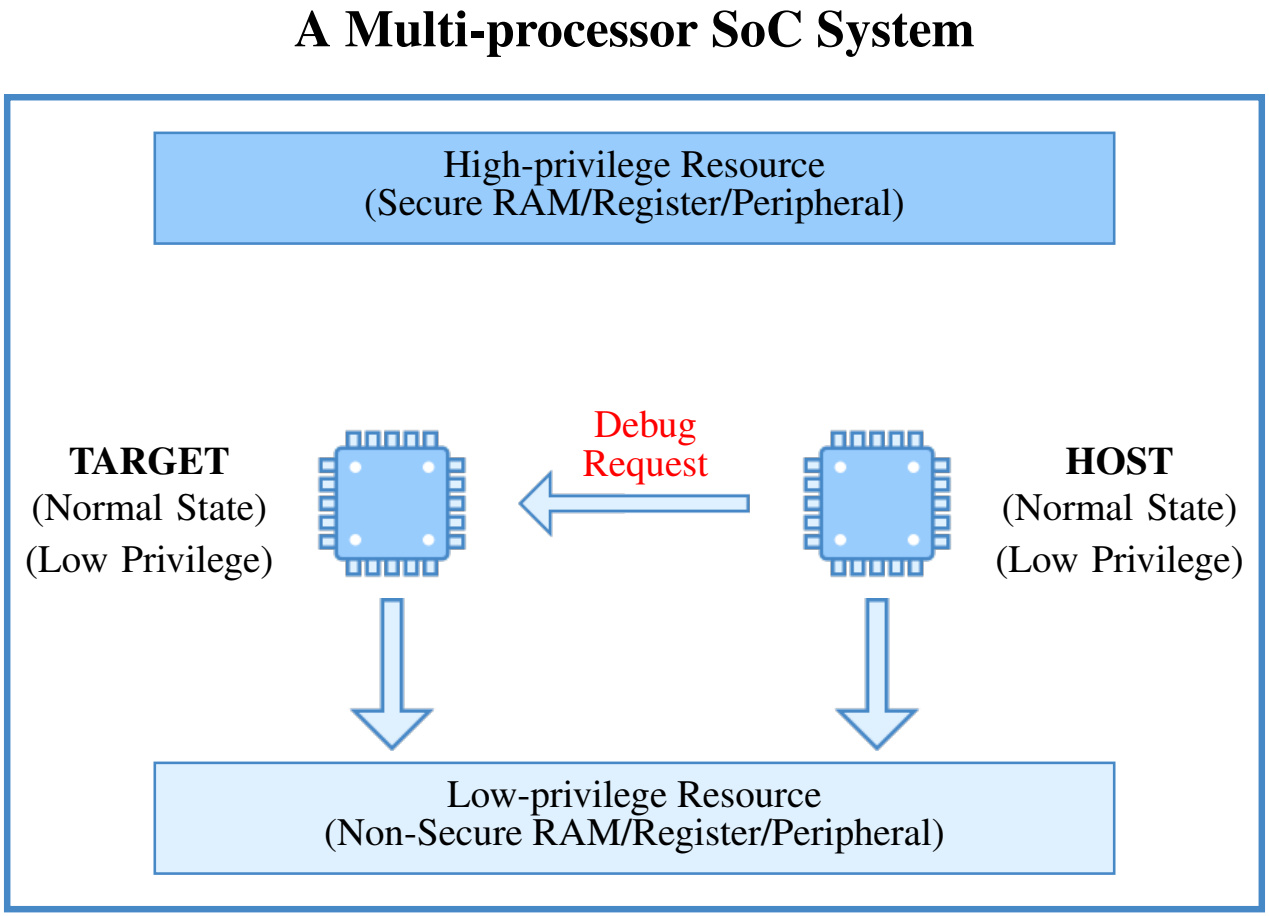
Nailgun Attack



Both processors are only access low-privilege resource.

- Normal state
- Low-privilege mode

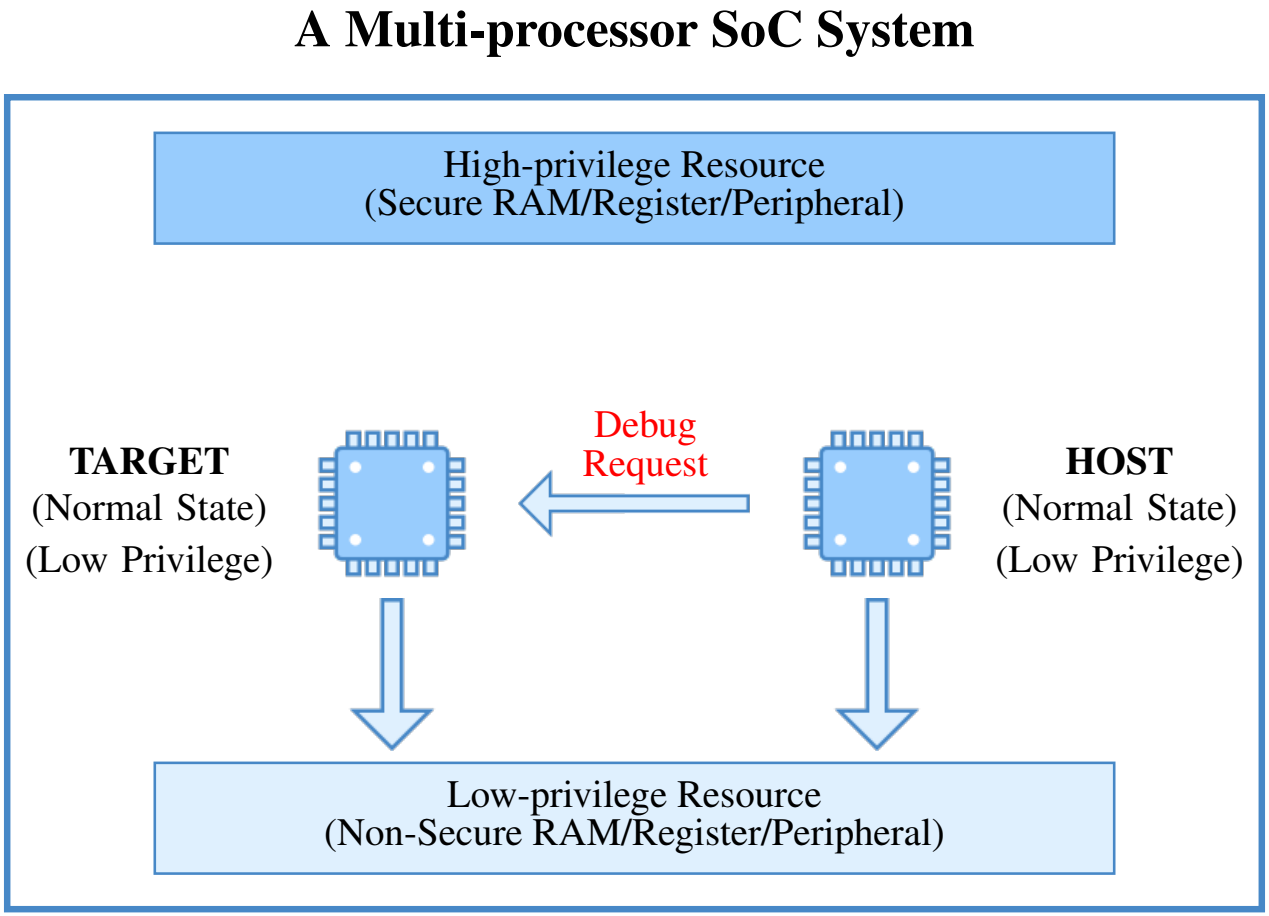
Nailgun Attack



`HOST` sends a **Debug Request** to `TARGET`,

- `TARGET` checks its authentication signal.
- Privilege of `HOST` is ignored.

Nailgun Attack



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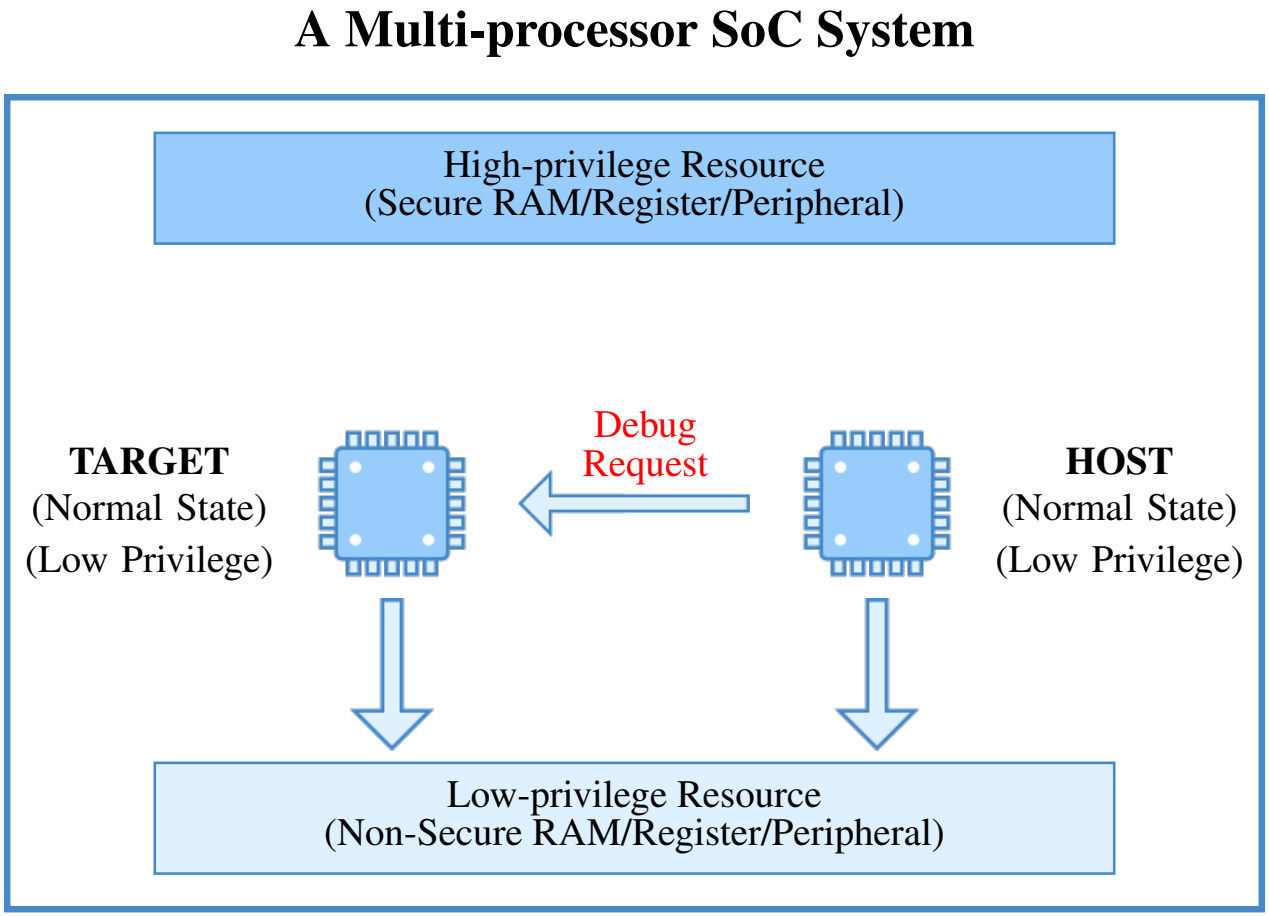
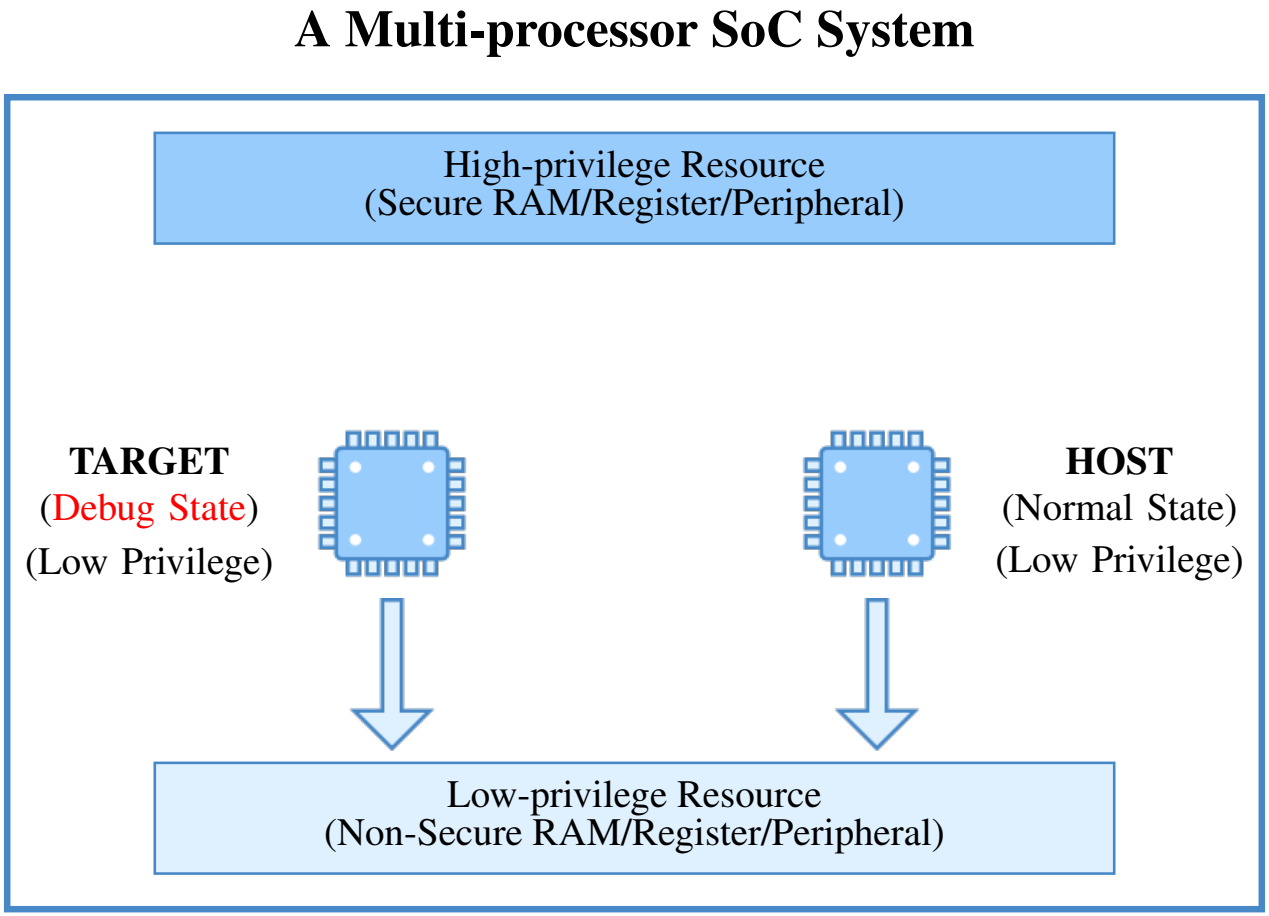


Implication: A low-privilege processor can make an arbitrary processor (even a high-privilege processor) enter the debug state.

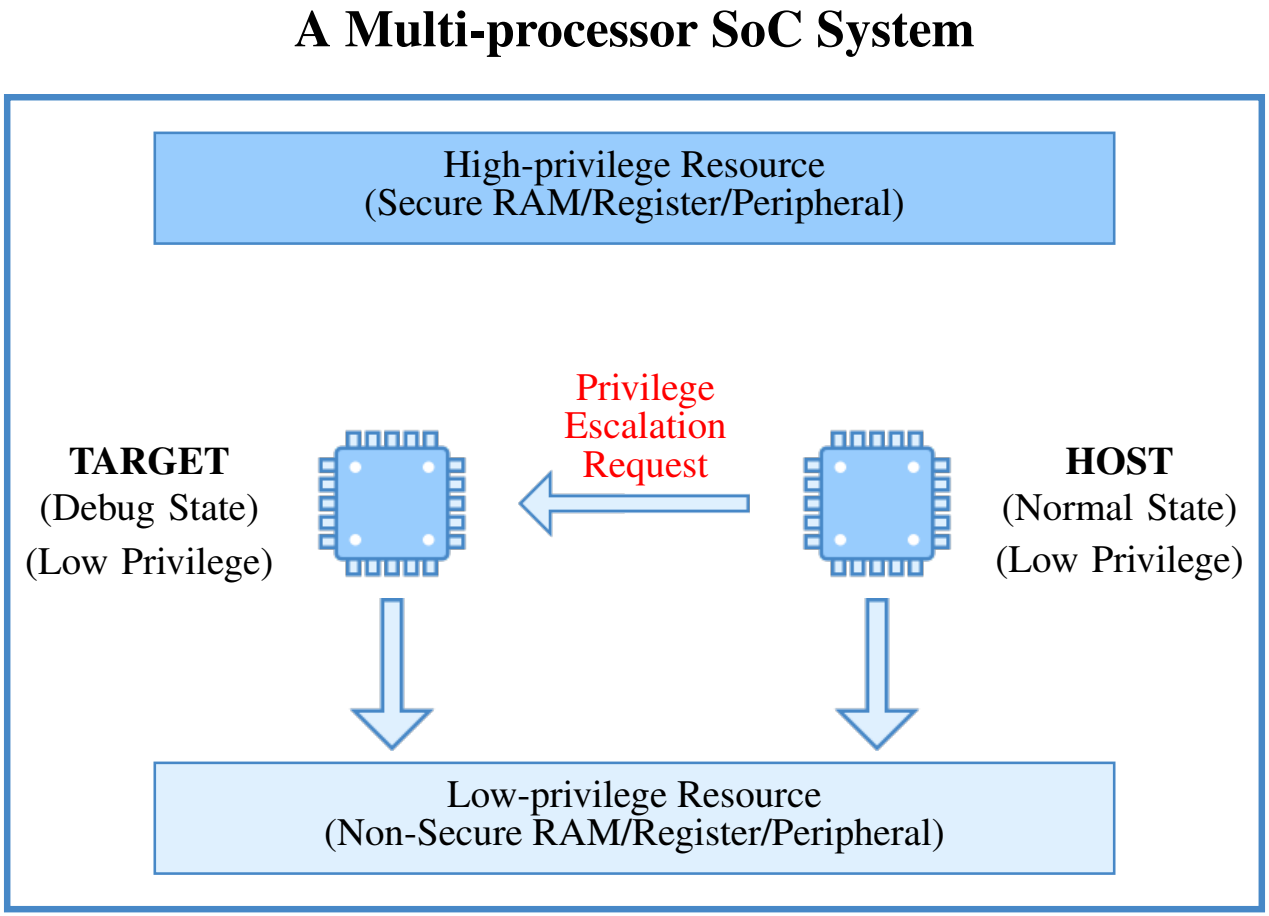
Nailgun Attack



`TARGET` turns to **Debug State** according to the request.

- Low-privilege mode
- No access to high-privilege resource

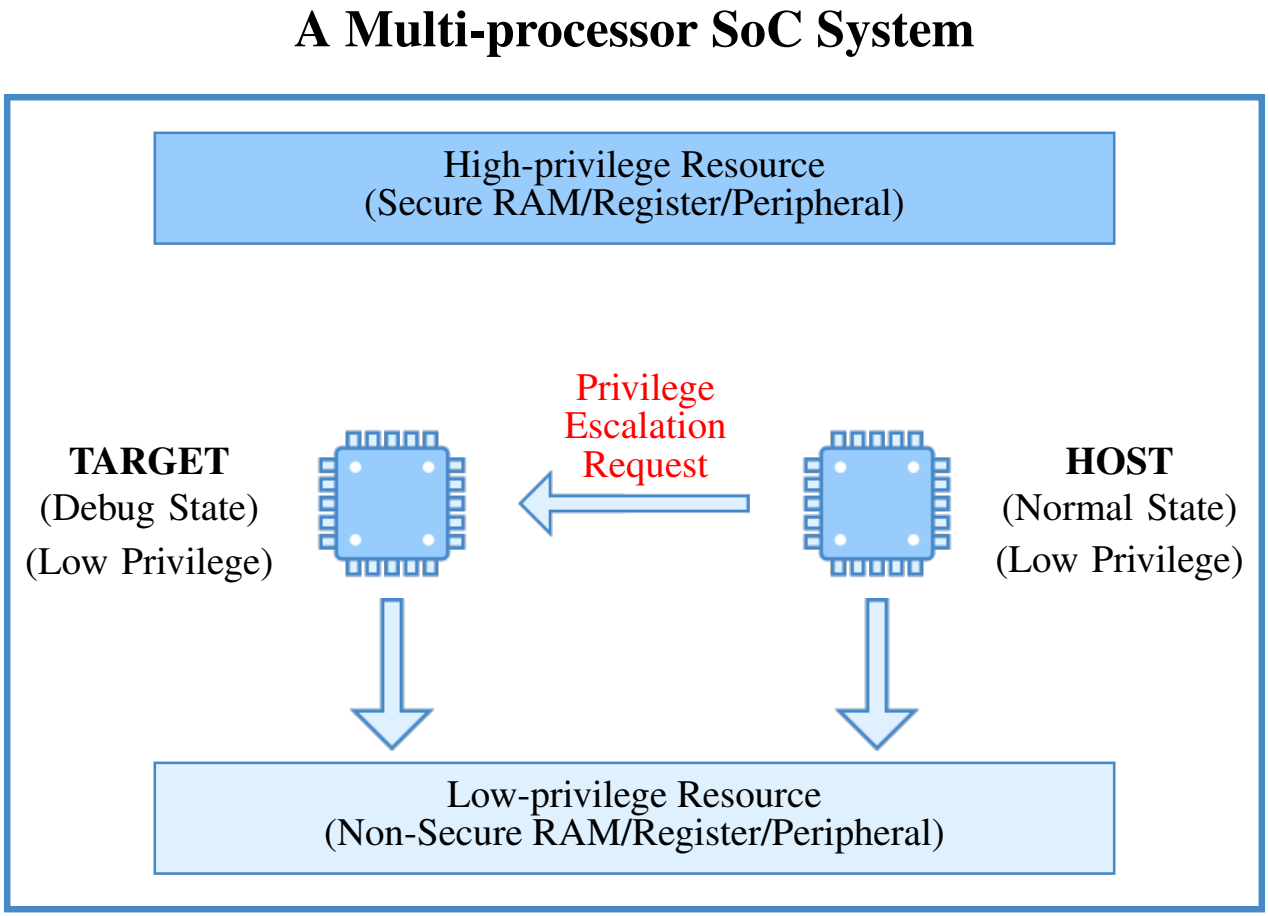
Nailgun Attack



`HOST` sends a **Privilege Escalation Request** to `TARGET`,

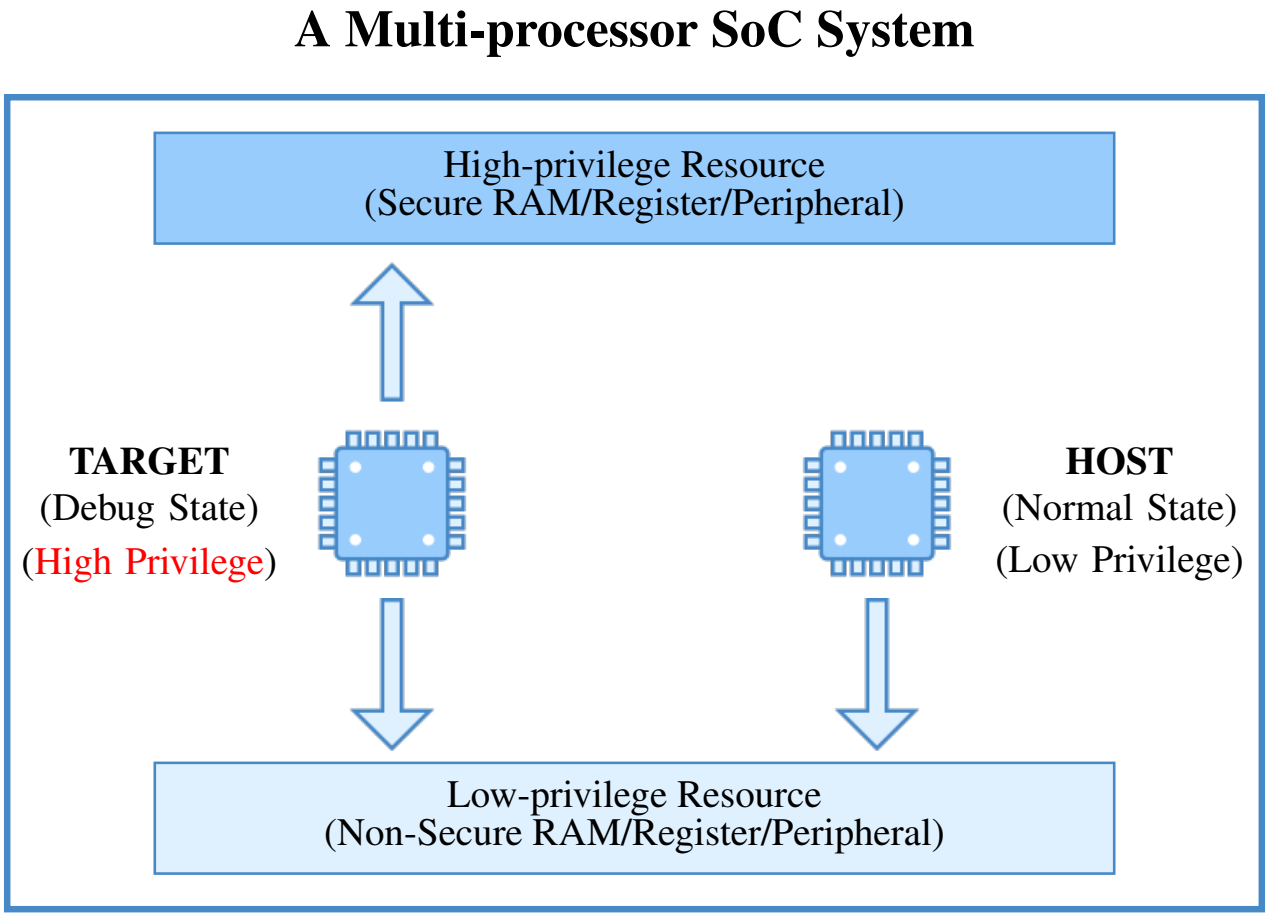
- E.g., executing `DCPS` series instructions.
- The instructions can be executed at any privilege level.

Nailgun Attack



Implication: The privilege escalation instructions enable a processor running in the debug state to gain a high privilege without restriction.

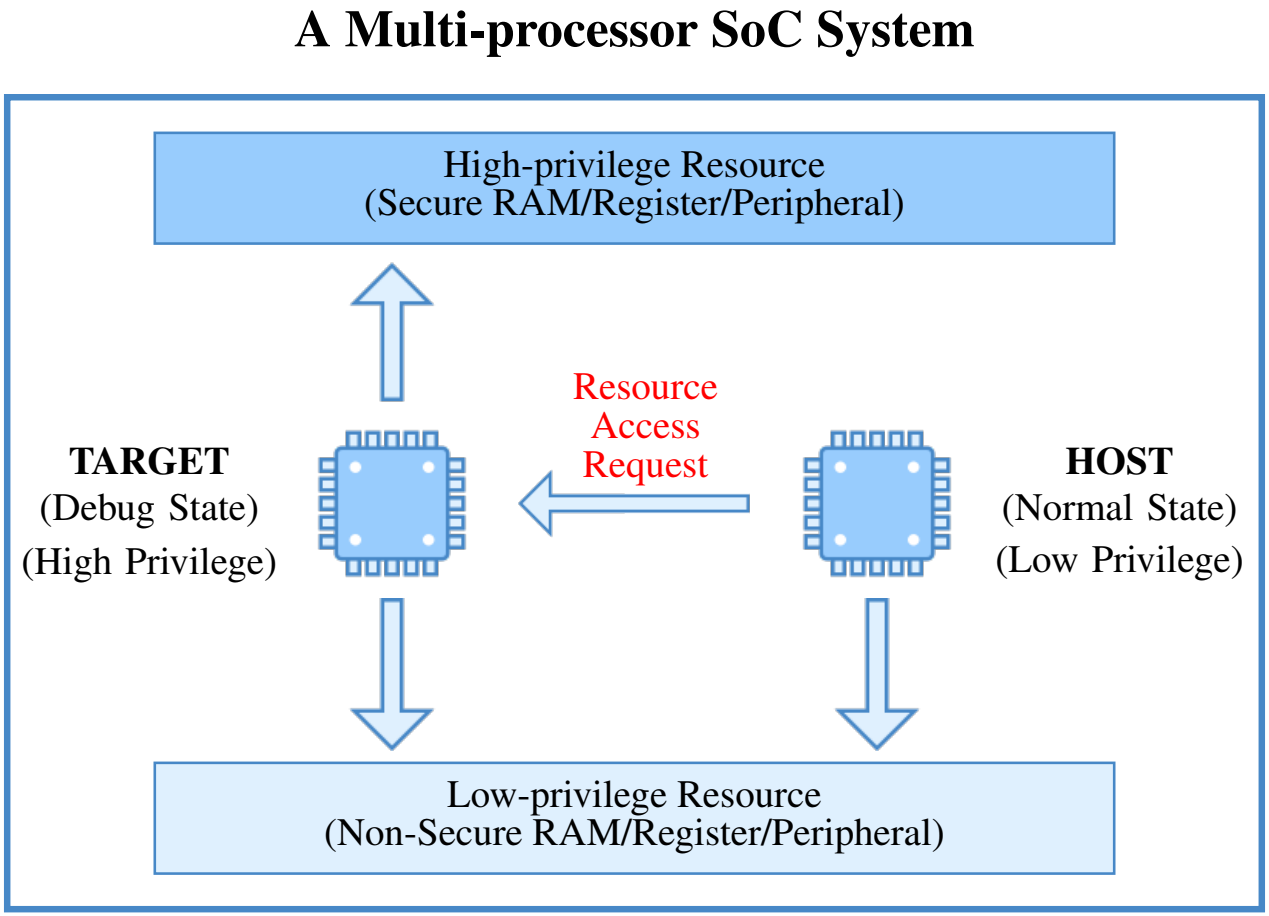
Nailgun Attack



`TARGET` turns to **High-privilege Mode** according to the request.

- Debug state, high-privilege mode
- Gained access to high-privilege resource

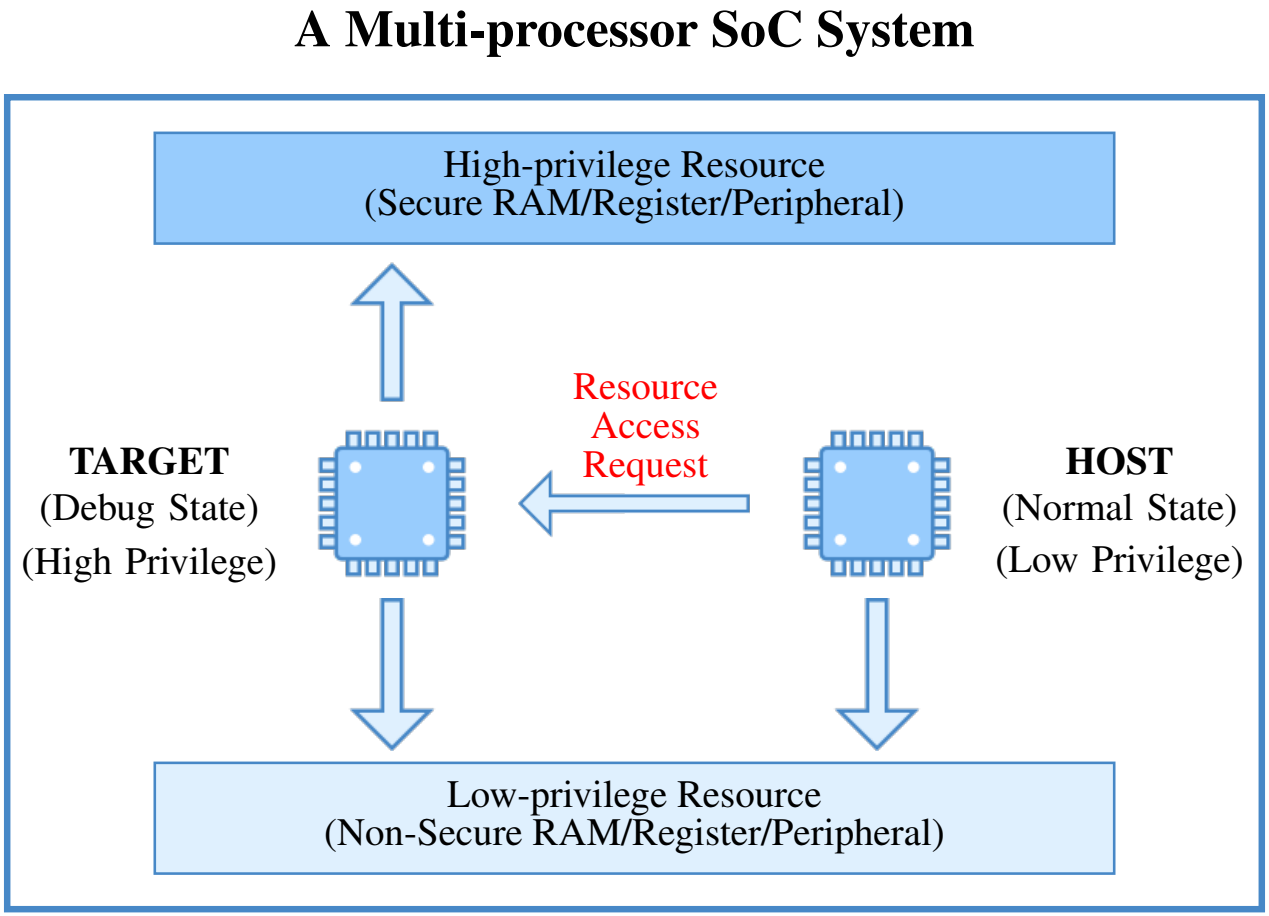
Nailgun Attack



`HOST` sends a **Resource Access Request** to `TARGET`,

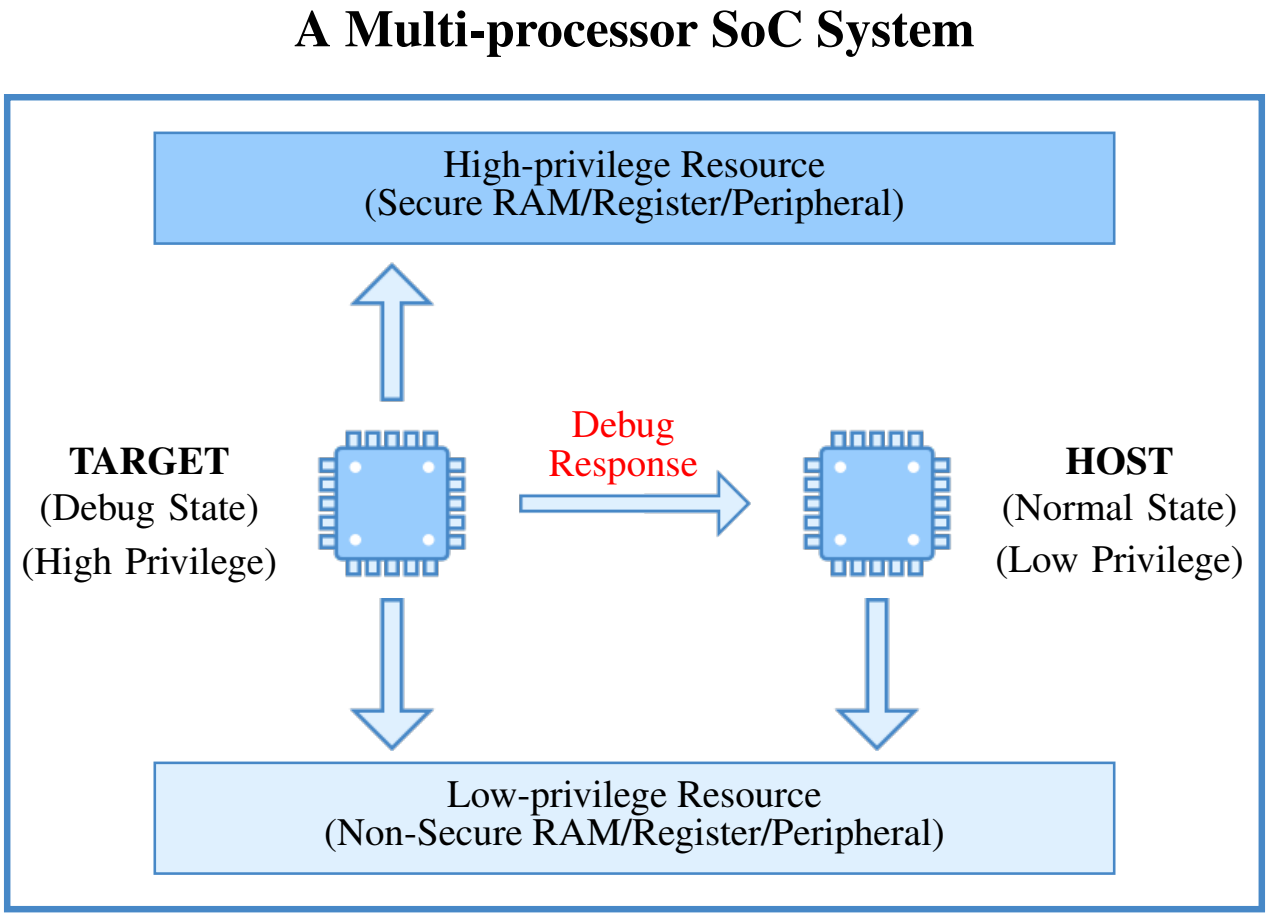
- E.g., accessing secure RAM/register/peripheral.
- Privilege of `HOST` is ignored.

Nailgun Attack



Implication: The instruction execution and resource access in `TARGET` does not take the privilege of `HOST` into account.

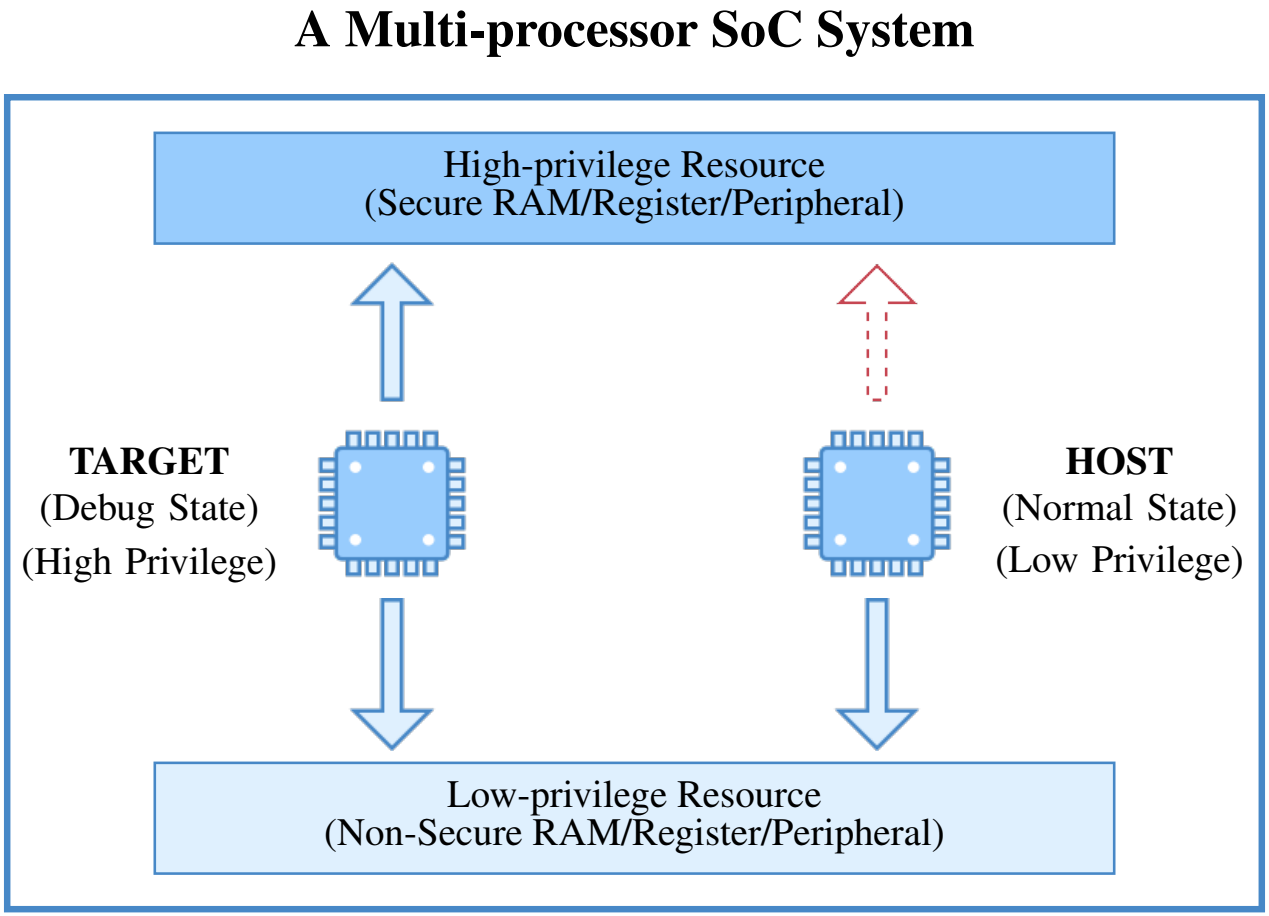
Nailgun Attack



`TARGET` return the result to `HOST`,

- i.e., content of the high-privilege resource.
- Privilege of `HOST` is ignored.

Nailgun Attack



`HOST` gains access to the high-privilege resource while running in,

- Normal state
- Low-privilege mode

Nailgun Attack

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Nailgun: Break the privilege isolation of ARM platform.

- Achieve access to high-privilege resource via misusing the ARM debugging features.
- Can be used to craft different attacks.

Attack Scenarios

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- Implemented Attack Scenarios:
  - Inferring AES keys from TrustZone.
  - Read Secure Configuration Register (SCR).
  - Arbitrary payload execution in TrustZone.
- Covered Architectures:
  - ARMv7, 32-bit ARMv8, and 64-bit ARMv8 architecture.
- Vulnerable Devices:
  - Development boards, IoT devices, cloud platforms, mobile devices.

Attack Scenarios

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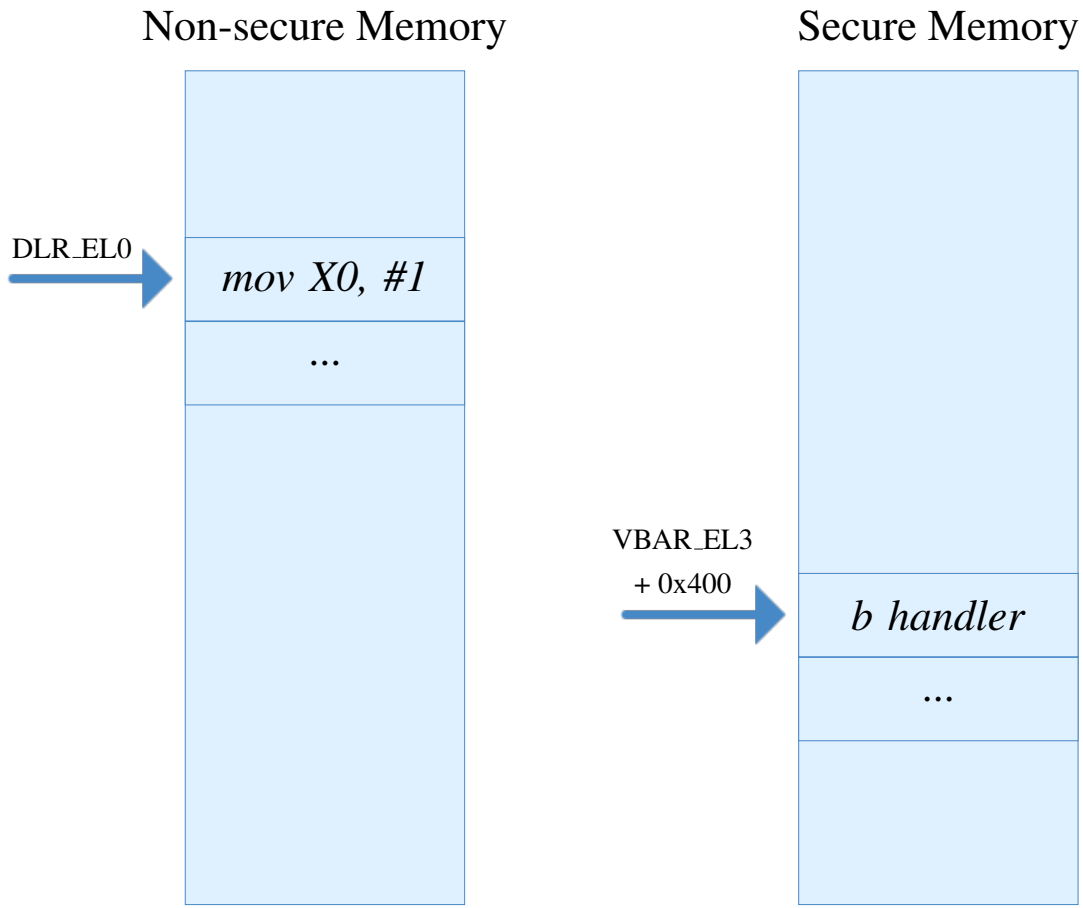
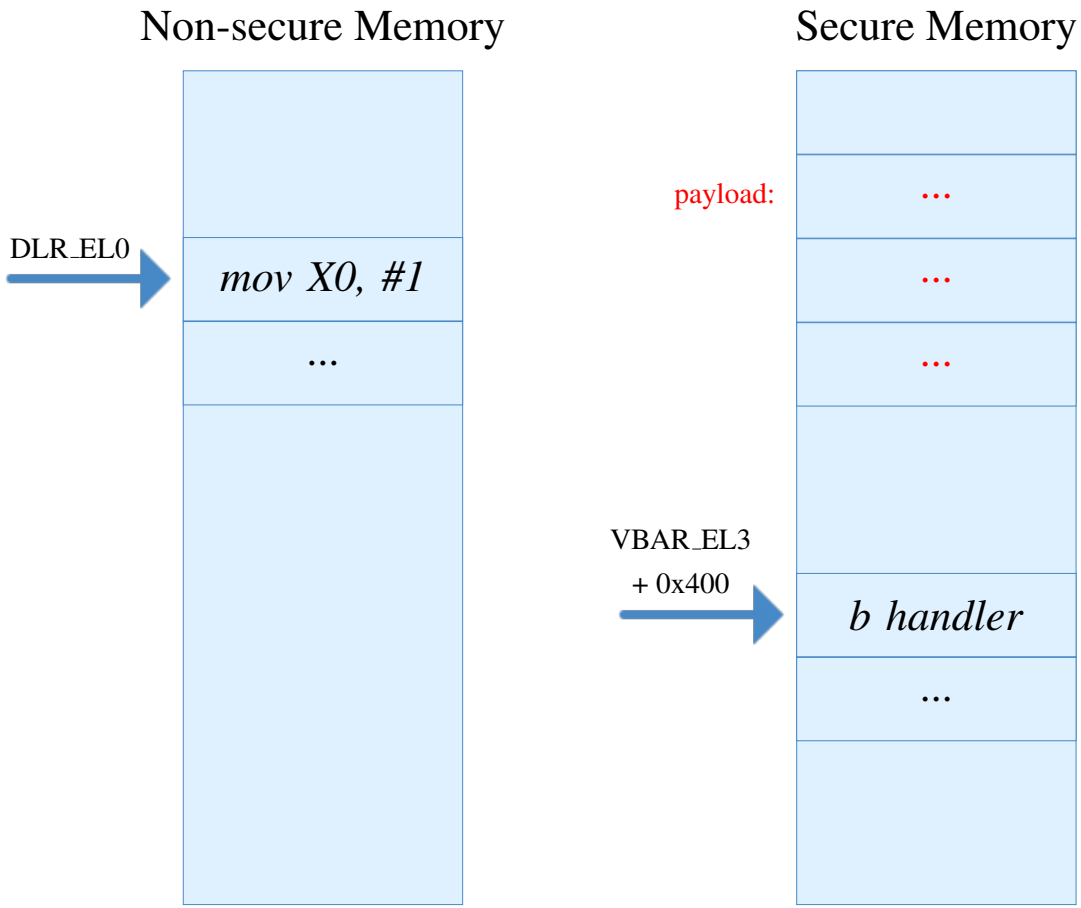
Arbitrary Code Execution in TrustZone



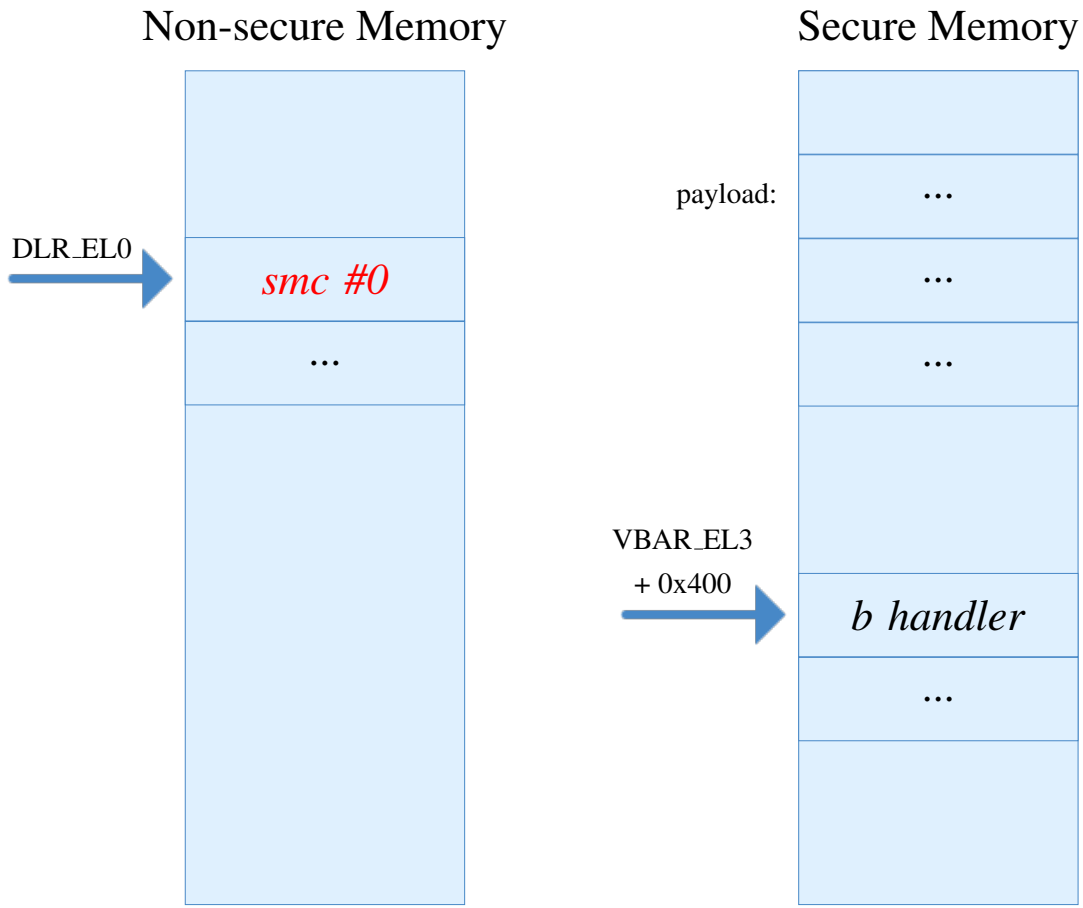
- *DLR_EL0* points to the debug return address.
- *VBAR_EL3* points to the exception vector in EL3.

Arbitrary Code Execution in TrustZone



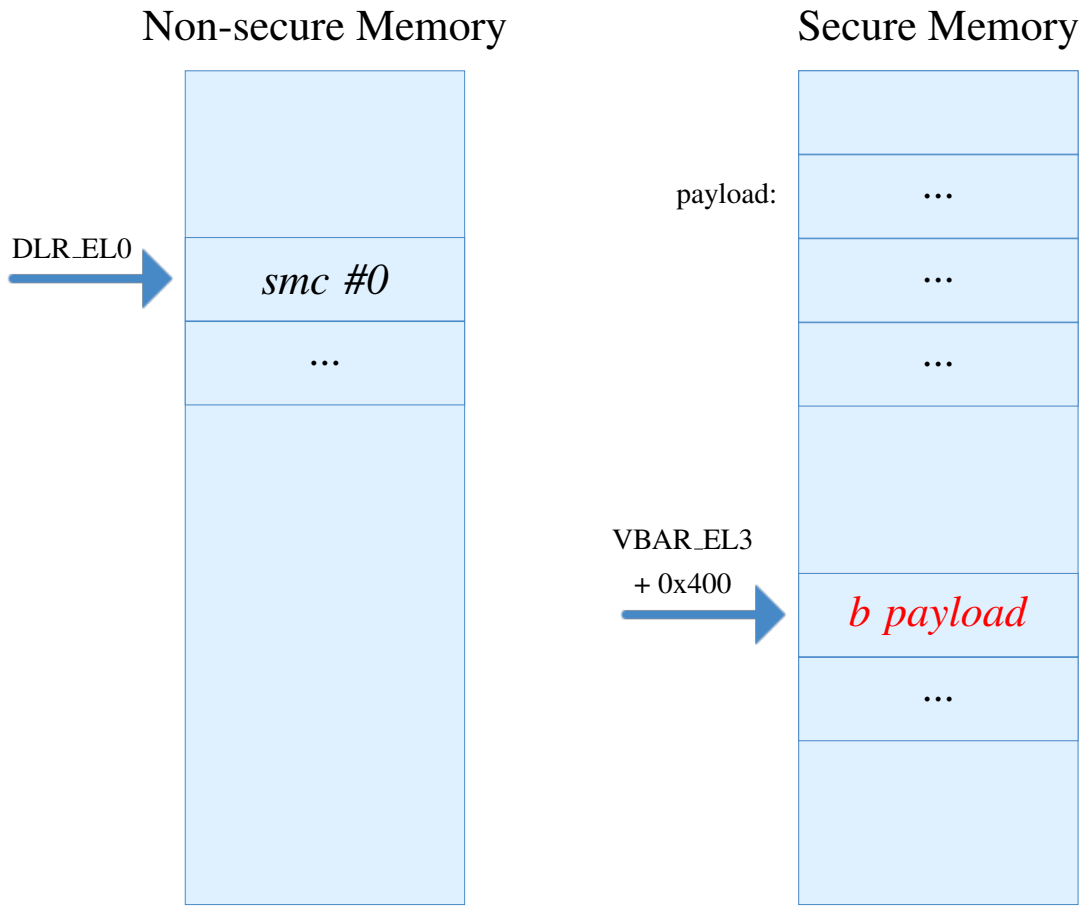
- With Nailgun, we can directly copy the payload to the secure memory.

Arbitrary Code Execution in TrustZone



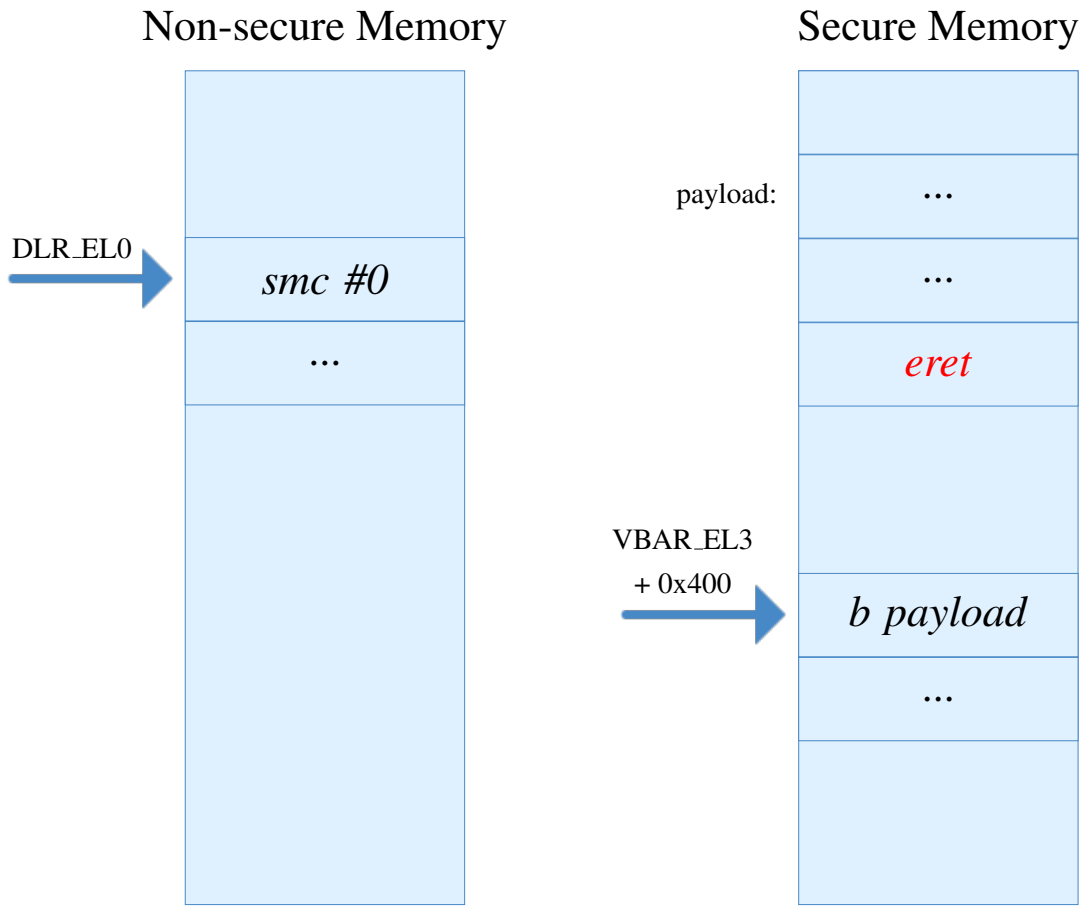
- Modify the instruction pointed by *DLR_EL0* to get into TrustZone.

Arbitrary Code Execution in TrustZone



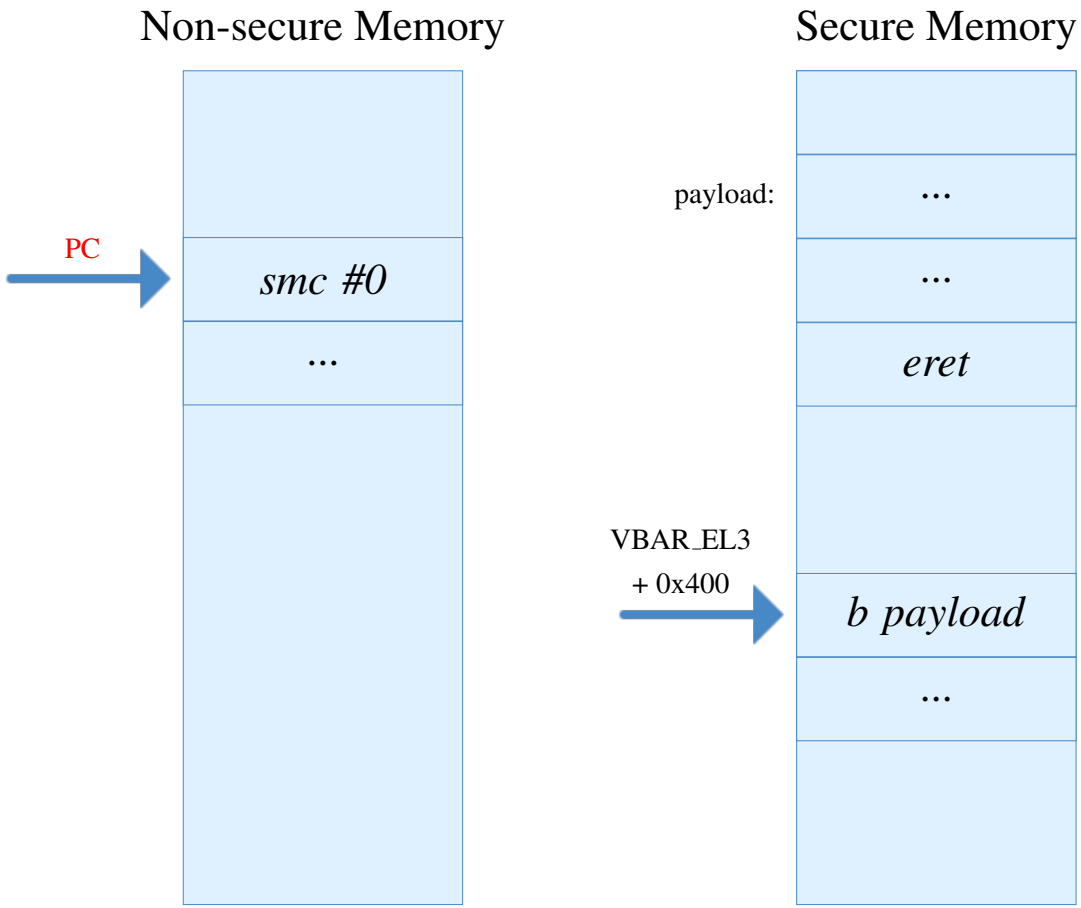
- Manipulate the exception vector to execute the payload while the SMC exception is routed to EL3.

Arbitrary Code Execution in TrustZone



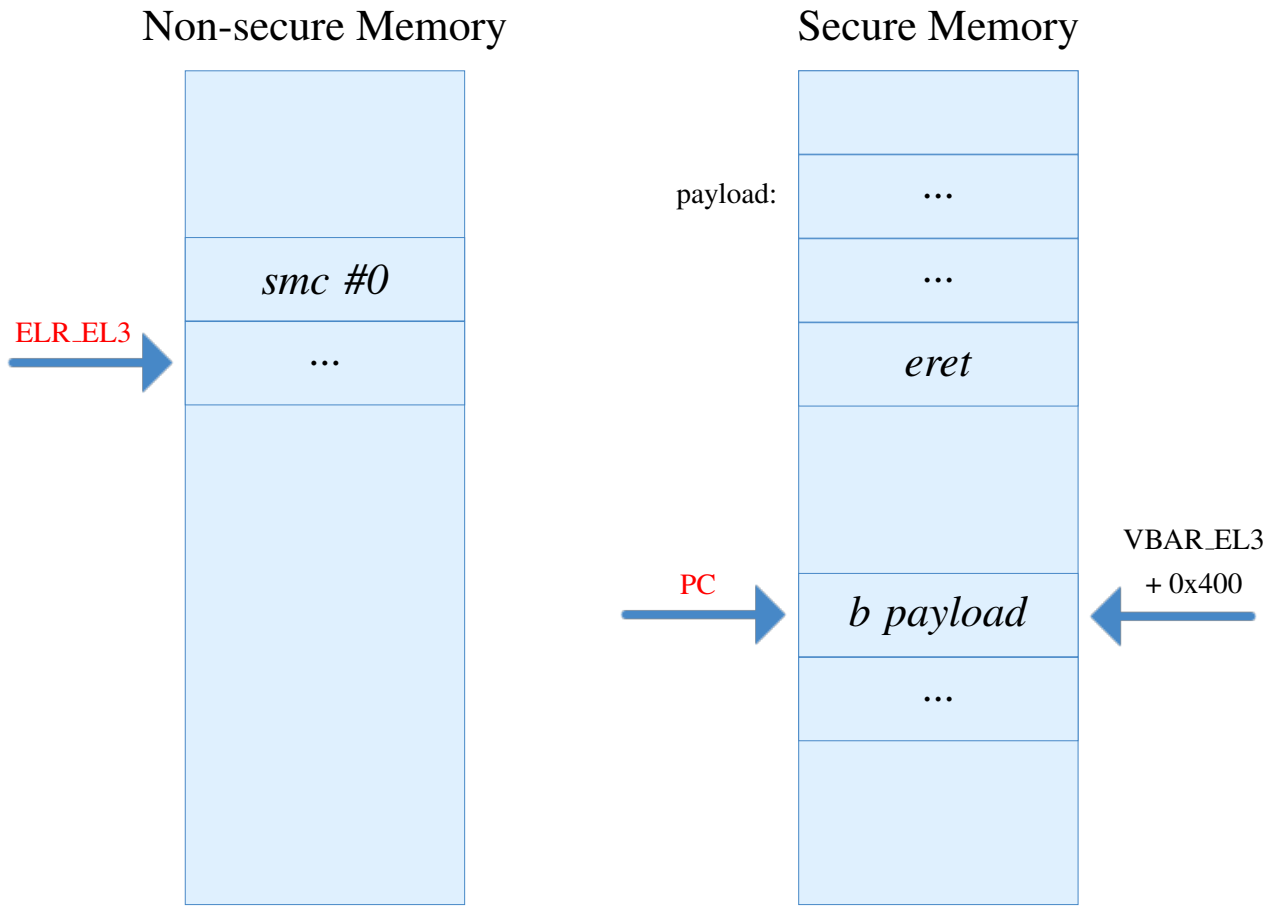
- The last instruction of the payload should be *eret*.

Arbitrary Code Execution in TrustZone



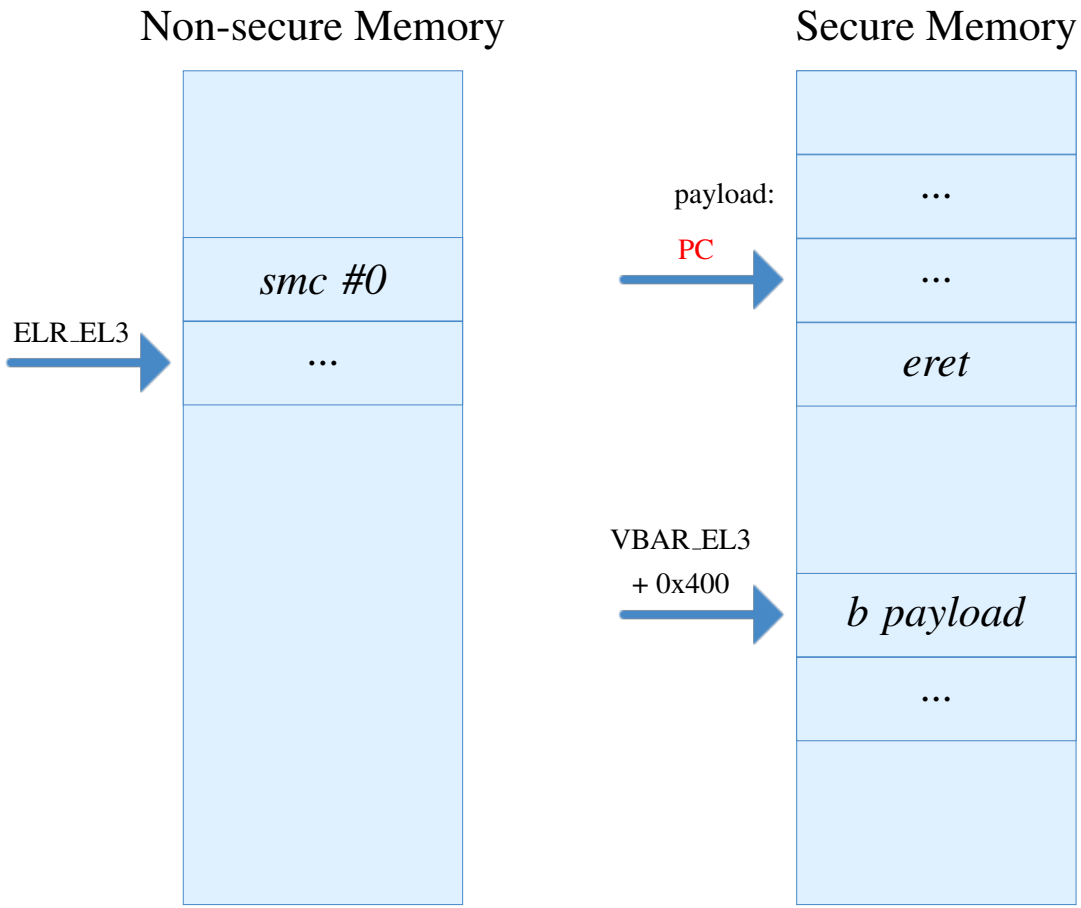
- Make `TARGET` exit the debug state.

Arbitrary Code Execution in TrustZone



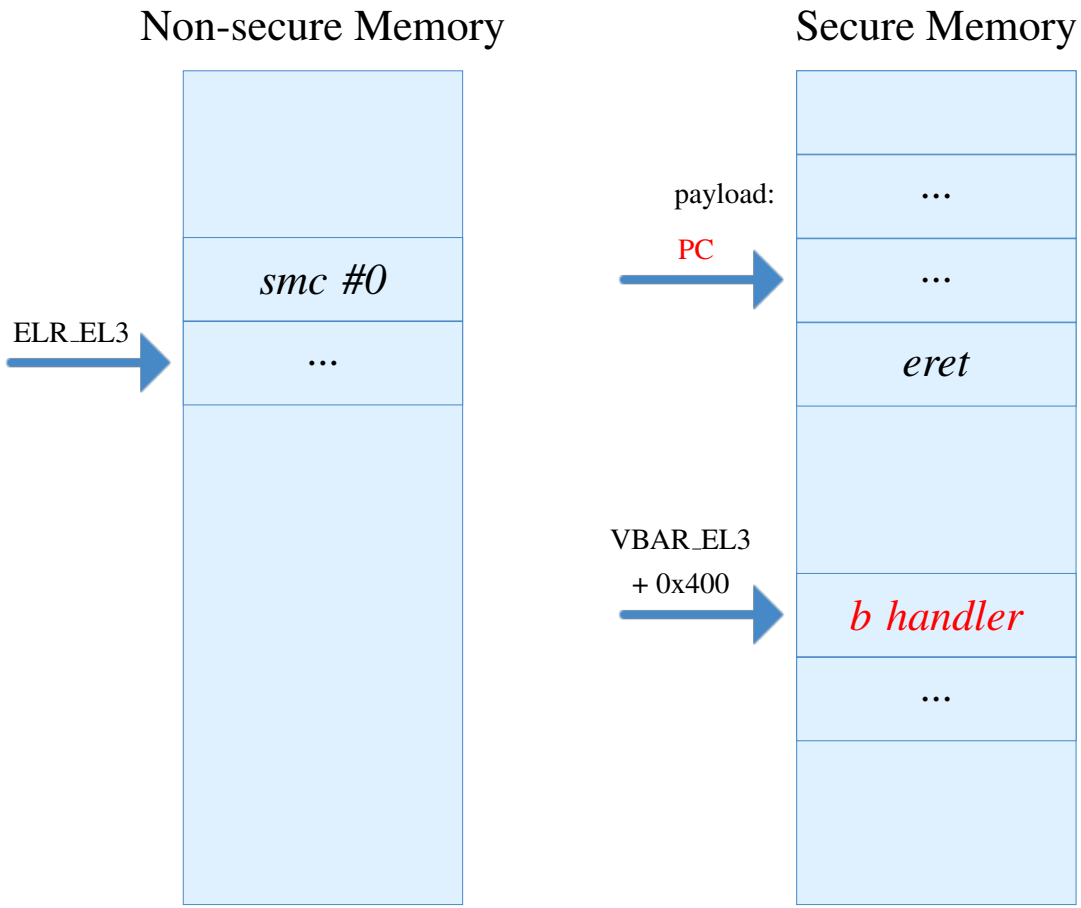
- *ELR_EL3* points to the exception return address.

Arbitrary Code Execution in TrustZone



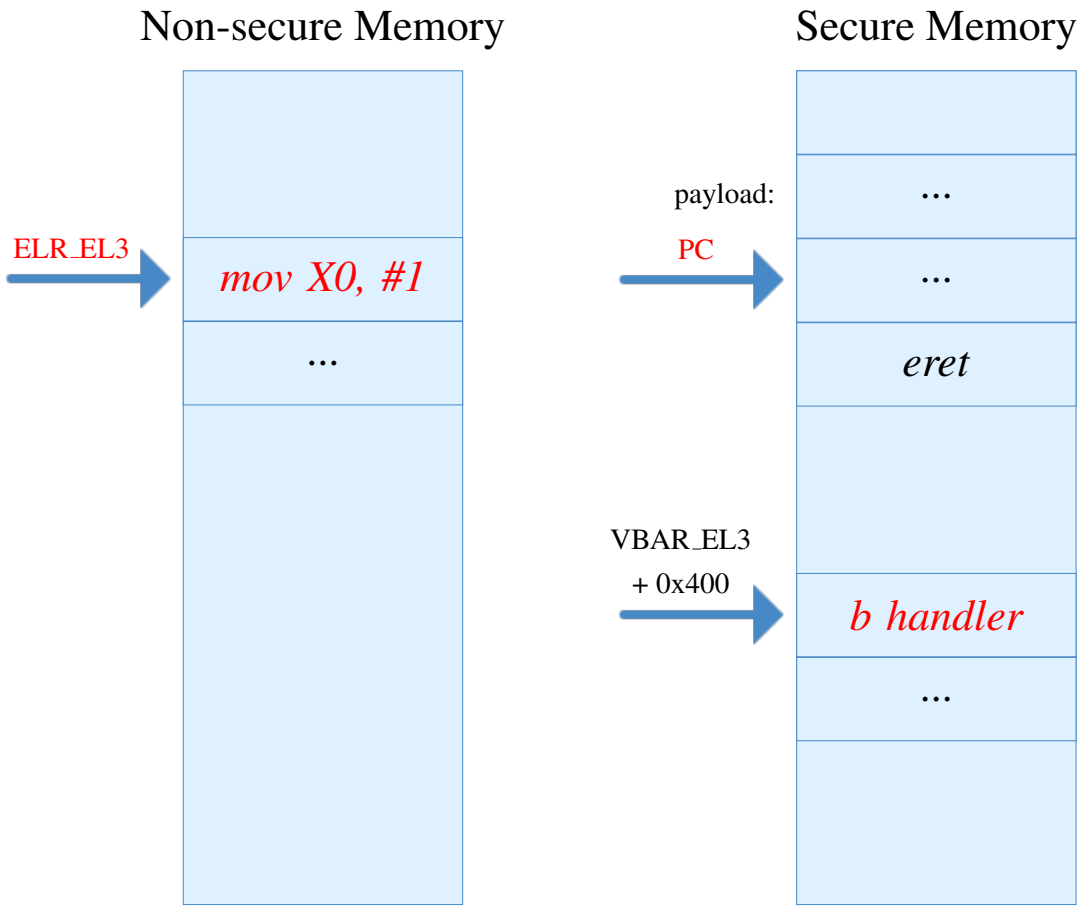
- The payload get executed.

Arbitrary Code Execution in TrustZone



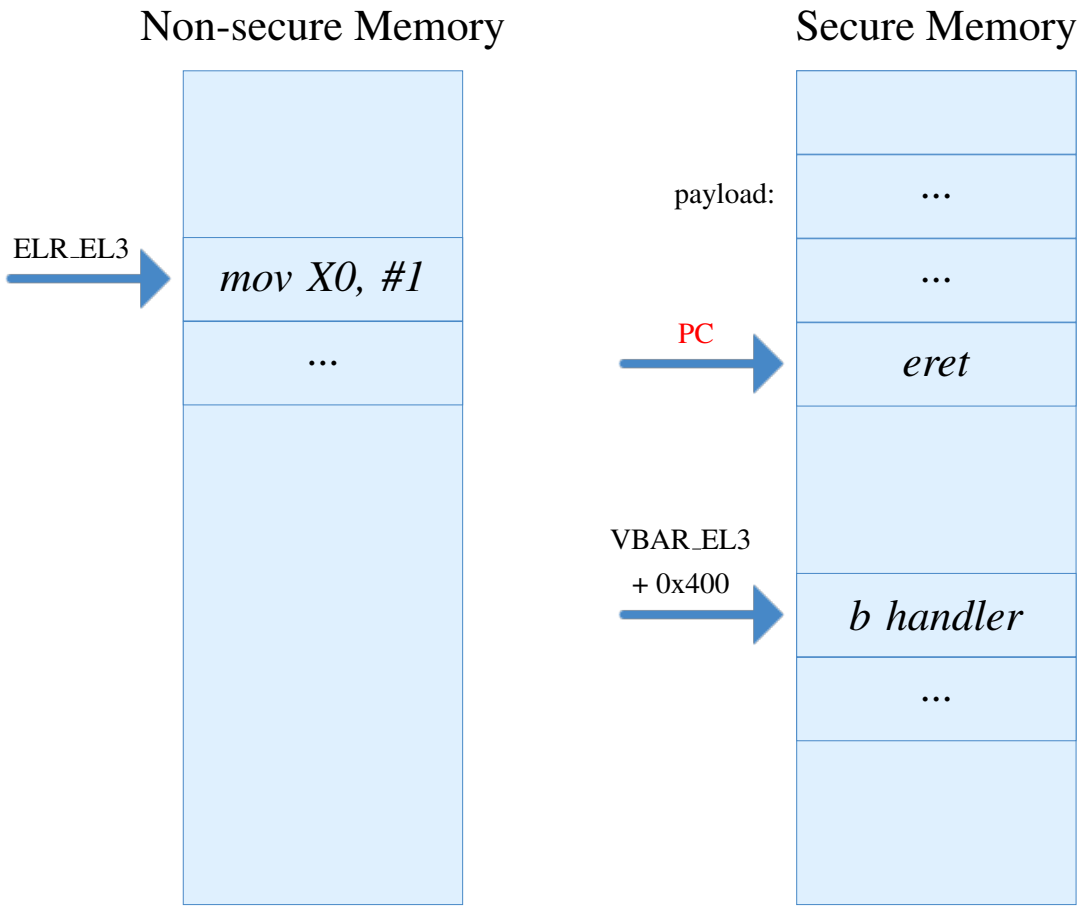
- In the payload, we first restore the exception vector.

Arbitrary Code Execution in TrustZone



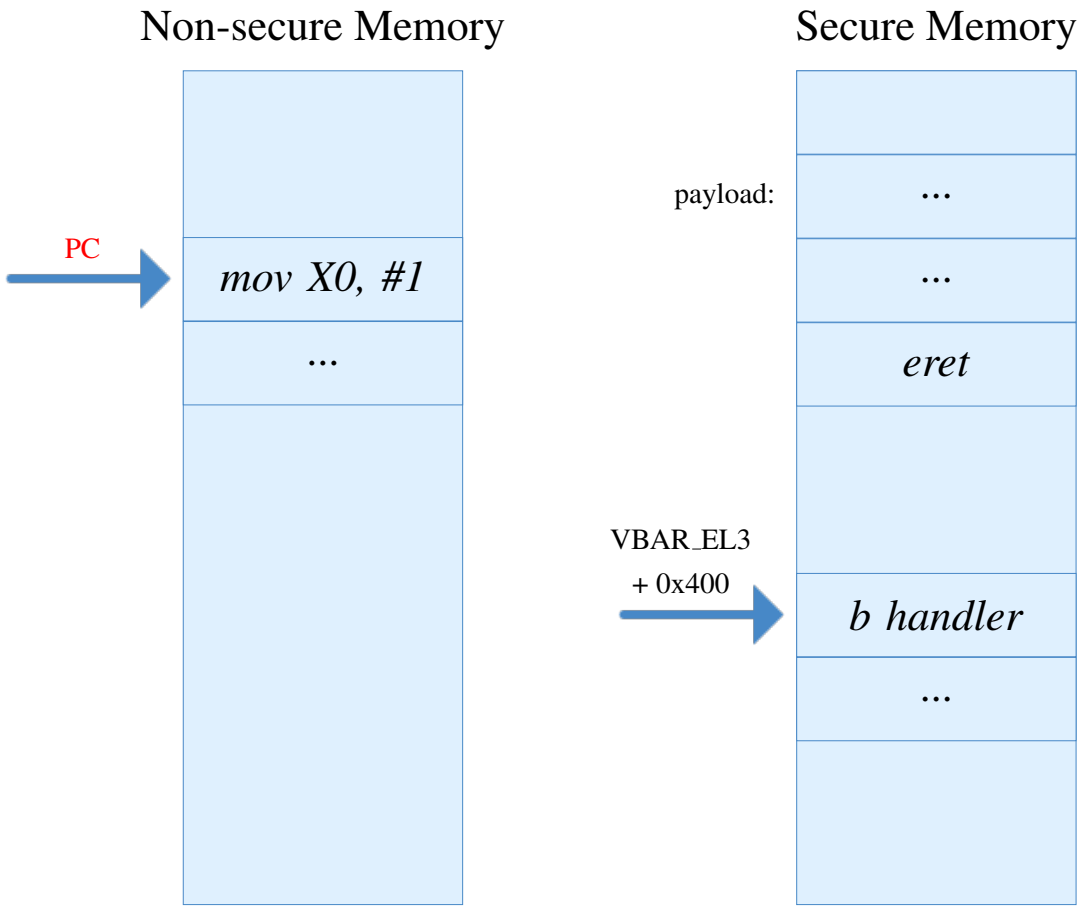
- Roll back the *ELR_EL3* register.
- Revert the modified instruction.

Arbitrary Code Execution in TrustZone



- The *eret* instruction will finish the exception handle process.

Arbitrary Code Execution in TrustZone



- After that, everything goes back to the original state.

Nailgun Attack

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Fingerprint extraction in commercial mobile phone.

- Deivce: Huawei Mate 7 (MT-L09)
- Firmware: MT7-L09V100R001C00B121SP05
- Fingerprint sensor: FPC1020

We choose this phone because the manual and driver of the fingerprint sensor is publicly available. Similar attack can be demonstrated on other devices with enabled debug authentication signals.

Nailgun Attack

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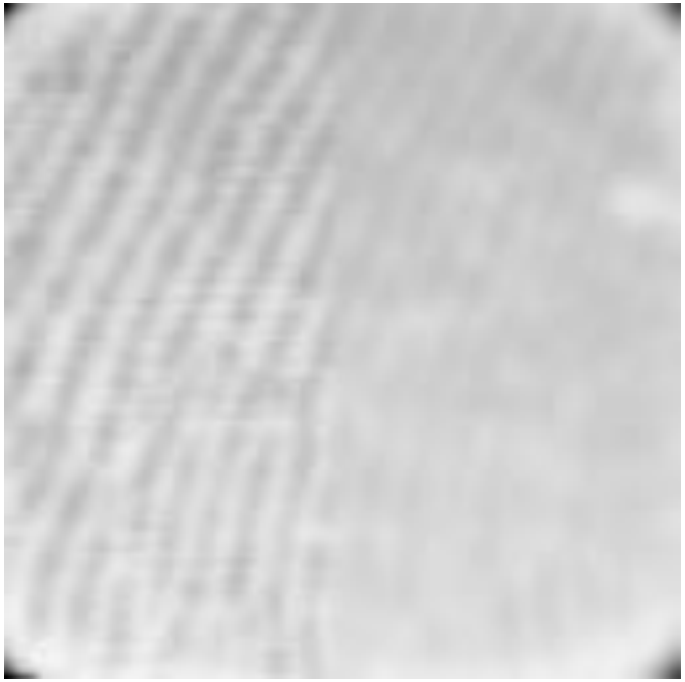
- Step 1: Learn the location of fingerprint data in secure RAM.
  - Achieved by reverse engineering.
- Step 2: Extract the data.
  - With the inter-processor debugging in Nailgun.
- Step 3: Restore fingerprint image from the extracted data.
  - Read the publicly available sensor manual.

Nailgun Attack



- The right part of the image is blurred for privacy concerns.
- Source code: `https://compass.cs.wayne.edu/nailgun/`
- The issue has been fixed in Huawei devices.

Nailgun Attack

Disclosure

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March 2018	Preliminary findings are reported to ARM
August 2018	Report to ARM and related OEMs with enriched result
October 2018	Issue is reported to MITRE
February 2019	PoCs and demos are released
April 2019	CVE-2018-18068 is released

Outline

WAYNE STATE UNIVERSITY

- Background
- Introduction
- Obstacles for Misusing the Traditional Debugging
- Nailgun Attack
- Mitigations
- Conclusion

Mitigations

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Simply disable the signals?

Mitigations

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Simply disable the authentication signals?

- Existing tools rely on the debug authentication signals.
  - E.g., [2, 3, 4, 5, 6, 7, 8, 9, 10, 11]
- Unavailable management mechanisms.
- OTP feature, cost, and maintenance.

Mitigations

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We suggest a comprehensive defense across different roles in the ARM ecosystem.

- For ARM, additional restriction in inter-processor debugging model.
- For SoC vendors, refined signal management and hardware-assisted access control to debug components.
- For OEMs and cloud providers, software-based access control.

Outline

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Conclusion

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- We present a study on the security of hardware debugging features on ARM platform.
- "Safe" components in legacy systems may be vulnerable in advanced systems.
- We suggest a comprehensive rethink on the security of legacy mechanisms.

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Thank you!

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Questions?

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Backup Slides

Nailgun in different ARM architecture

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- 64-bit ARMv8 architecture: ARM Juno r1 board.
  - Embedded Cross Trigger (ECT) for debug request.
  - Binary instruction to Instruction Transfer Register (ITR).
- 32-bit ARMv8 architecture: Raspberry PI Model 3 B+.
  - Embedded Cross Trigger (ECT) for debug request.
  - First and last half of binary instruction should be reversed in ITR.
- ARMv7 architecture: Huawei Mate 7.
  - Use Debug Run Control Register for debug request.
  - Binary instruction to Instruction Transfer Register (ITR).

Instruction Execution in Debug State

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In normal state, `TARGET` is executing instructions pointed by `pc`

Instruction Execution in Debug State

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In debug state, `TARGET` stops executing the instruction at `pc`

Instruction Execution in Debug State

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In debug state, write binary instruction to ITR for execution

Instruction Execution in Debug State

WAYNE STATE UNIVERSITY

In debug state, write binary instruction to ITR for execution

Instruction Execution in Debug State

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In debug state, write binary instruction to ITR for execution